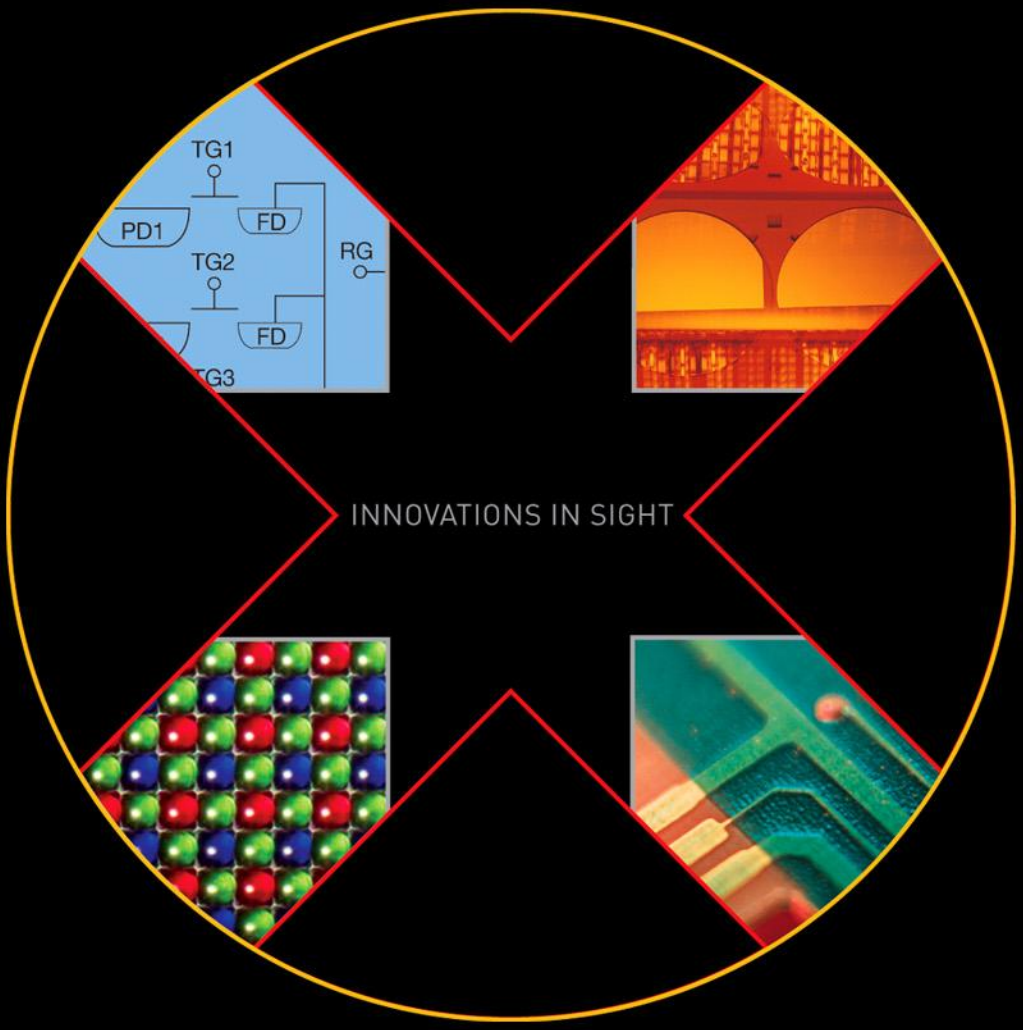
DEVICE PERFORMANCE SPECIFICATION

Revision 4.0 MTD/PS-0415

April 27, 2010



KODAK KAF-0261 IMAGE SENSOR

512 (H) X 512 (V) FULL FRAME CCD COLOR IMAGE SENSOR

Kodak
Image Sensor Solutions

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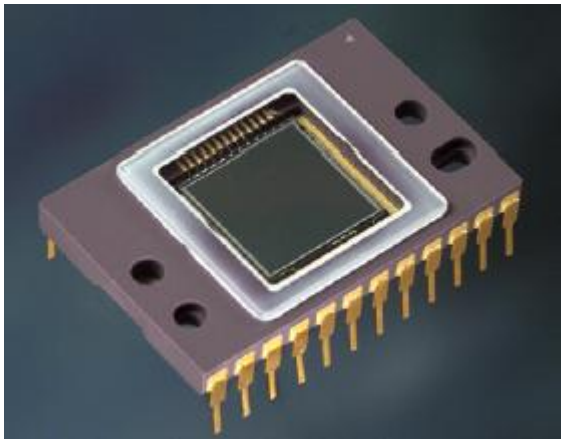
SUMMARY SPECIFICATION

KODAK KAF-0261 IMAGE SENSOR

512 (H) X 512 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

The KODAK KAF-0261 Image Sensor is a high performance, charge coupled device (CCD) designed for a wide range of image sensing applications in the 0.3µm to 1.1µm wavelength band. The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard polysilicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths. The low dark current of the KAF-0261 makes this device suitable for low light imaging applications without sacrificing in charge capacity. The clock selectable on-chip output amplifiers have been specially designed to meet two different needs. The first is a high sensitivity 2-stage output with 10µV/e- charge to voltage conversion ratio. The second is a single stage output with 3.5µV/e- charge to voltage conversion ratio.



Parameter	Typical Value
Architecture	Full Frame CCD
Number of Active Pixels	512 (H) x 512 (V)
Pixel Size	20 µm (H) x 20 µm (V)
Active Image Size	10.2 mm (H) x 10.2 mm (V)
Chip Size	11.3 mm (H) x 11.6 mm (V)
Optical Fill Factor	100%
Output Sensitivity High Sensitivity Output High Dynamic Range Output	 10 µV/electron 2.0 µV/electron
Saturation Signal High Sensitivity Output High Dynamic Range	 200,000 electrons 500,000 electrons
Readout Noise (1 MHz)	22 electrons rms
Dark Current (25° C, Accumulation Mode)	<30 pA/cm2
Dark Current Doubling Rate	6 °C
Dynamic Range (Sat Sig/Dark Noise) High Sensitivity Output	83 dB
High Dynamic Range Output Range	87 dB
Quantum Efficiency (450, 550, 650 nm)	35%, 55%, 58%
Maximum Data Rate High Sensitivity Output High Dynamic Range Output	 5 MHz 2 MHz
Transfer Efficiency	>0.99997
Package	CERDIP Package
Cover Glass	Clear or AR coated, 2 sides

FEATURES

- Front Illuminated Full-Frame Architecture
- 512(H) x 512(V) Photosensitive Pixels
- Transparent Gate True Two Phase Technology (Enhanced Spectral Response)
- 20µm (H) x 20µm (V) Pixel Size
- 1:1 Aspect Ratio with 100% Fill Factor
- Single Readout Register
- 2 Clock Selectable Outputs
- High Gain Output (10 µV/e-) for low noise, Low Gain Output (3.5 µV/e-) for high dynamic range
- Low Dark Current (<30pA/cm2 at T=25° C)

APPLICATIONS

- Scientific Imaging

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ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0808	KAF- 0261-AAA-CD-BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	KAF- 0261-AAA S/N
4h0809	KAF- 0261-AAA-CD-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0810	KAF- 0261-AAA-CP-BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade	
4H0811	KAF- 0261-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0081	KEK-4H0081-KAF-0261-12-5	Evaluation Board (Complete Kit)	N/A

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE

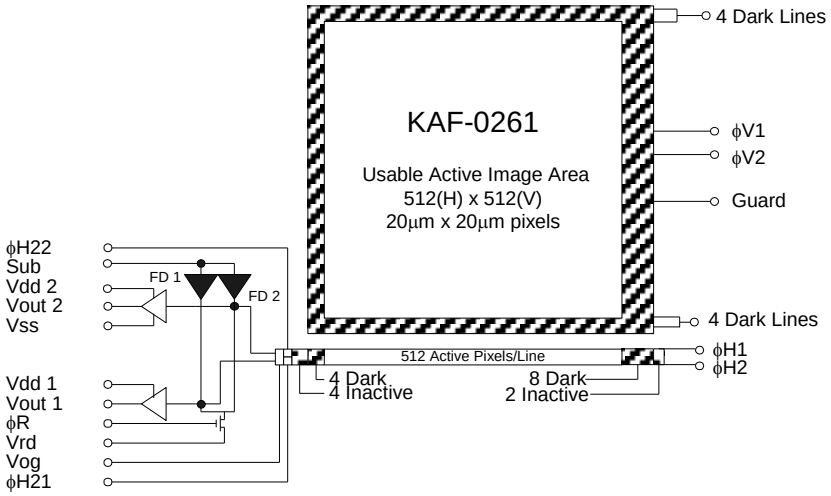

Figure 1: Block Diagram

Shaded areas represent 4 non-imaging pixels at the beginning and 8 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

The KAF-0261 consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. (See Figure 1) Both registers incorporate two-phase buried channel CCD technology. The vertical register consists of 20µm x 20µm photocapacitor sensing elements (pixels) that also serves as the transport mechanism. The pixels are arranged in a 512(H) x 512(V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. There is no storage array, so this device must be synchronized with strobe illumination or shuttered during readout.

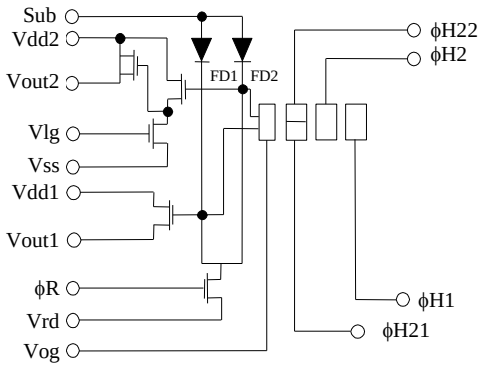

Figure 2: Output Structure

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Output Structure

The final gate of the horizontal register is split into two sections, ϕH21 and ϕH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), tie ϕH22 to a negative voltage to block charge transfer, and tie ϕH21 to ϕH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), tie ϕH21 to a negative voltage and ϕH22 to ϕH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression Vfd= Q/Cfd.

The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

IMAGE ACQUISITION

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

CHARGE TRANSPORT

Integrated charge is transported to the output in a two step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram illustration in section 2.7, integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to horizontal CCD begins when ϕV1 is brought high causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate. ϕV1 and ϕV2 now reverse their polarity causing the charge packets to 'spill' forward under the ϕV2 gate of the next pixel. The rising edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel. The sequence completes when ϕV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using ϕH1 and ϕH2 pins) as shown. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which is buffered by the output amplifier. The cycle repeats until all lines are read.

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PHYSICAL DESCRIPTION

Pin Description and Device Orientation

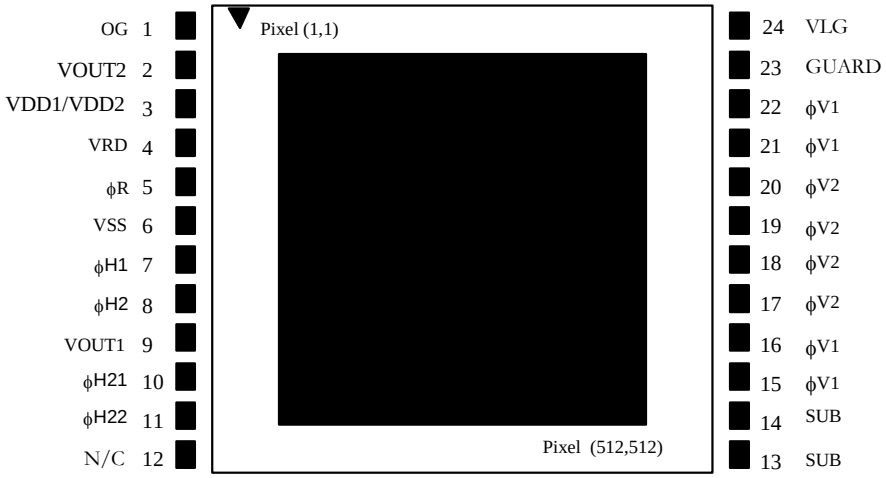

Figure 3: Pinout Diagram

Pin	Name	Description
1	OG	Output Gate
2	VOUT2	Video Output from High Sensitivity Two-Stage
3	VDD1/VDD2	Amplifier Supply for VOUT1 and VOUT2 amplifiers
4	VRD	Reset Drain
5	ϕR	Reset Clock
6	VSS	Output Amplifier Return
7	ϕH1	Horizontal (Serial) CCD Clock - Phase 1
8	ϕH2	Horizontal (Serial) CCD Clock - Phase 2
9	VOUT1	Video Output from High Dynamic Range Single-Stage Amplifier
10	ϕH21	Last Horizontal (Serial) CCD Phase - Split Gate
11	ϕH22	Last Horizontal (Serial) CCD Phase - Split Gate
12	N/C	No Connection

Pin	Name	Description
24	VLG	First Stage Load Transistor Gate for Two-Stage
23	GUARD	Guard Ring
22	ϕV1	Vertical (Parallel) CCD Clock - Phase 1
21	ϕV1	Vertical (Parallel) CCD Clock - Phase 1
20	ϕV2	Vertical (Parallel) CCD Clock - Phase 2
19	ϕV2	Vertical (Parallel) CCD Clock - Phase 2
18	ϕV2	Vertical (Parallel) CCD Clock - Phase 2
17	ϕV2	Vertical (Parallel) CCD Clock - Phase 2
16	ϕV1	Vertical (Parallel) CCD Clock - Phase 1
15	ϕV1	Vertical (Parallel) CCD Clock - Phase 1
14	VSUB	Substrate
13	VSUB	Substrate

Notes:

1. Pins 15, 16, 21, and 22 must be connected together - only one Phase 1-clock driver is required
2. Pins 17, 18, 19, and 20 must be connected together - only one Phase 2-clock driver is required

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IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to voltage, multiply by the amplifier sensitivity.

SPECIFICATIONS

Electro-Optical

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Optical Fill Factor	F F		100		%		
Photoresponse Non-uniformity	PRNU			5	% rms	Full Array	die[10]
Quantum Efficiency (450, 550, 650 nm)	QE					See Q.E. curve (Figure 6)	design[11]

CCD Parameters Common to Both Outputs

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Sat. Signal - Vccd register	Ne-sat	450	500		ke-	2	design[11]
Dark Current	Jd		15.3 400	30 750	pA/cm2 e-pixel/sec	25 C (mean of all pixels)	die[10]
Dark Current Doubling Temp	DCDR	5	6.3	7.5	oC		design[11]
Dark Signal Non-uniformity	DSNU			750	e-/pix/sec	4	die[10]
Charge Transfer Efficiency	CTE		.99997			5	die[10]
Photoresponse Non-Linearity	PRNL		1	2	%	9	
Blooming Suppression	Bs		none				

CCD Parameters Specific to High Gain Output Amplifier

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Output Sensitivity	Vout/Ne-	9	10		uV/electron		design[11]
Sat. Signal	N_{e^-sat}	180	200	240	ke-	1	design[11]
Total Sensor Noise	n_{e^-total}		13	20	e- rms	7	design[11]
Horizontal CCD Frequency	F_H		2	5	MHz	6	design[11]
Dynamic Range	DR	79	83		dB	8	design[11]

CCD Parameters Specific to Low Gain (High Dynamic Range) Output Amplifier

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Output Sensitivity	Vout/Ne-	3.2	3.5		uV/electron		design[10]
Sat. Signal	N_{e^-sat}	550K	628K		ke-	3	design[11]
Total Sensor Noise	n_{e^-total}		22	30	e- rms	7	die[10]
Horizontal CCD Frequency	F_H		0.5	2	MHz	6	design[11]
Dynamic Range	DR	85	87		dB	8	design[11]

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Notes:

1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register.
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 16 sub arrays (128 x 128) exceed the maximum dark current specification.
5. For 2MHz data rate and T = 30 C to -40 C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
7. At Tintegration = 0; data rate = 1 MHz; temperature = -30 C.
8. Uses 20LOG(Ne- sat / ne- total) where Ne- sat refers to the appropriate saturation signal.
9. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.

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TYPICAL PERFORMANCE CURVES

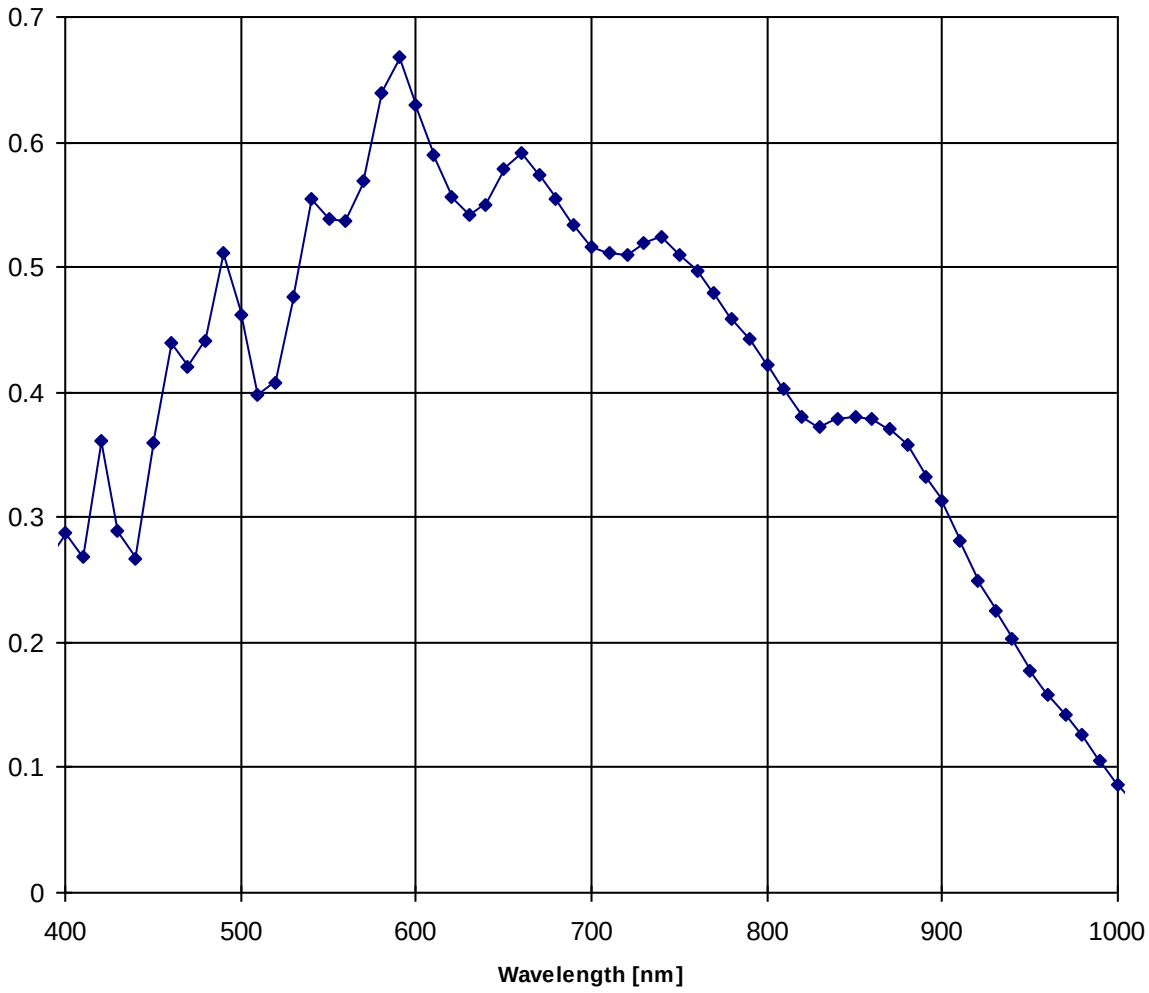


Figure 4: Typical Spectral Response

DEFECT DEFINITIONS

SPECIFICATIONS

Point Defect	Cluster Defect	Column Defect
10	4	0

Dark Defects A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation

Bright Defect A pixel whose dark current exceeds 4500 electrons/pixel/second at 25ºC

Cluster Defect A grouping of not more than 5 adjacent point defects

Column Defect A grouping point defects along a single column. (Dark Column)

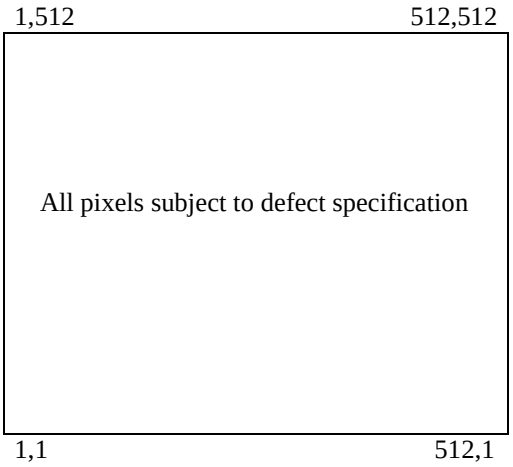
A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25 C. (Bright Column)

A column that does not exhibit the minimum charge capacity specification. (Low charge capacity)

A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)

Neighboring Pixels The surrounding 128 x 128 pixels of ± 64 columns/rows

Defects are separated by no less than 3 pixels in any one direction.



OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Voltage	All Clocks	-16	+16	V	1
Voltage	OG	0	+8	V	2
Voltage	VRD, VSS, VDD, GUARD	0	+20	V	2
Current	Output Bias Current (IDD)		10	mA	
Capacitance			10	pF	

Notes:

1. Voltage between any two clocks or between any clock and Vsub.
2. Voltage with respect to Vsub.

Warning:

For maximum performance, built-in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage. Devices are rated as Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test.)

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DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Pin Impedance
Substrate	VSUB	0.0	0.0	0.0	V	Common
Output Amplifier Supply	VDD	15.0	+17.0	17.5	V	5 pf, 2KΩ (Note 1)
Output Amplifier Return	VSS	1.4	+2.0	2.1	V	5 pf, 2KΩ
Reset Drain	VRD	11.5	+12	12.5	V	5 pf, 1MΩ
Output Gate	OG	4.0	4.5	5.0	V	5 pf, 10MΩ
Guard Ring	GUARD	9.0	+10.0	15.0	V	350 pF, 10MΩ
Load Gate	VLG	VSS - 1.0	VSS	VSS + 1.0	V	

Notes:

1. Vdd = 17 volts for applications where the expected output voltage > 2.0 volts. For applications where the expected useable output voltage is < 2 volts Vdd can be reduced to 15 volts.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Pin Impedance
Vertical Clock - Phase 1	ϕV1	Low	-10.2	-10.0	-9.0	V	13 nf, 10MΩ
Vertical Clock - Phase 1	ϕV1	High	0.0	0	2.0	V	
Vertical Clock - Phase 2	ϕV2	Low	-10.2	-10.0	-9.0	V	16 nf, 10MΩ
Vertical Clock - Phase 2	ϕV2	High	0.0	0	2.0	V	
Horizontal Clock - Phase 1	ϕH1	Low	-2.2	-2.0	-1.8	V	160 pf, 10MΩ
Horizontal Clock - Phase 1	ϕH1	High	7.8	+8.0	8.2	V	
Horizontal Clock - Phase 2	ϕH2	Low	-2.2	-2.0	-1.8	V	110 pf, 10MΩ
Horizontal Clock - Phase 2	ϕH2	High	7.8	+8.0	8.2	V	CØh1-h2 = 75pf
Reset Clock	ϕR	Low	2.0	3.0	3.5	V	10 pF, 10MΩ
Reset Clock	ϕR	High		10.0		V	

			Using the High Gain Output (Vout2)			Using the High Dynamic Range Output (Vout1)				
Description	Symbol	Level	Min	Nom	Max	Min	Nom	Max	Units	Pin Impedance
Horizontal Clock - Phase 1	ϕH21	Low	-4	ϕH2 low	ϕH2 low		ϕH2		V	10pF, 10MΩ
Horizontal Clock - Phase 1	ϕH21	High	-4	ϕH2 low	ϕH2 low		ϕH2		V	
Horizontal Clock - Phase 2	ϕH22	Low		ϕH2		-4	ϕH2 low	ϕH2 low	V	10pF, 10MΩ
Horizontal Clock - Phase 2	ϕH22	High		ϕH2		-4	ϕH2 low	ϕH2 low	V	

Notes:

1. When using Vout1 ϕH21 is clocked identically with ϕH2 while ϕH22 is held at a static level. When using Vout2 ϕH21 and ϕH22 are exchanged so that ϕH22 is identical to ϕH2 and ϕH21 is held at a static level. The static level should be the same voltage as ϕH2 low.

2. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.

3. ϕV1,2 capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.

4. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

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TIMING

REQUIREMENTS AND CHARACTERISTICS

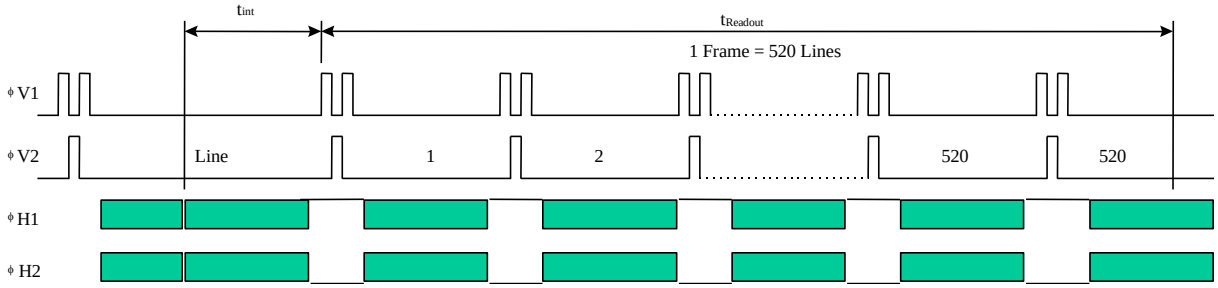
Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		5	8	MHz	1, 2, 3
V1, V2 Clock Frequency	f_V		100	125	kHz	1, 2, 3
Pixel Period (1 Count)	tpix	125	200		ns	
ϕH1, ϕH2 Set-up Time	$t_{\phi HS}$	500	1000		ns	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	4	5		µs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	40	64		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	78	122		µs	7

Notes:

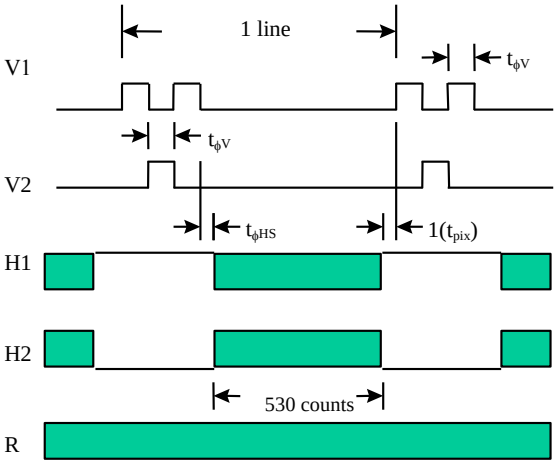
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously
5. $t_{readout} = (520 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise
7. $t_{line} = (3 * t\phi V) + t\phi HS + 530* t_{pix} + t_{pix}$

Note: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult Eastman Kodak in those situations, which require special consideration.

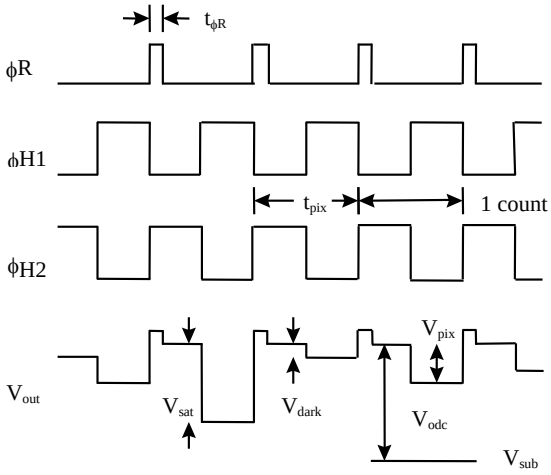
Frame Timing



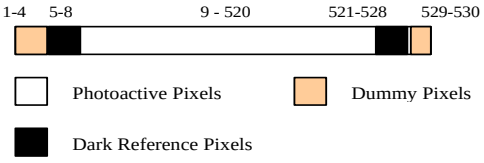
Line Timing Detail



Pixel Timing Detail



Line Content



V_{sat}	Saturated pixel video output signal
V_{dark}	Video output signal in no light situation, not zero due to Jdark
V_{pix}	Pixel video output signal level, more electrons =more negative
V_{odc}	Video level offset with respect to vsub
V_{sub}	Analog Ground

* See Image Aquisition section

Figure 5: Timing Diagrams

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-100	+80	ºC	At Device
Operating Temperature	T_{OP}	-70	+50	ºC	At Device

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices".

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.
6. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370ºC. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

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MECHANICAL INFORMATION

COMPLETED ASSEMBLY

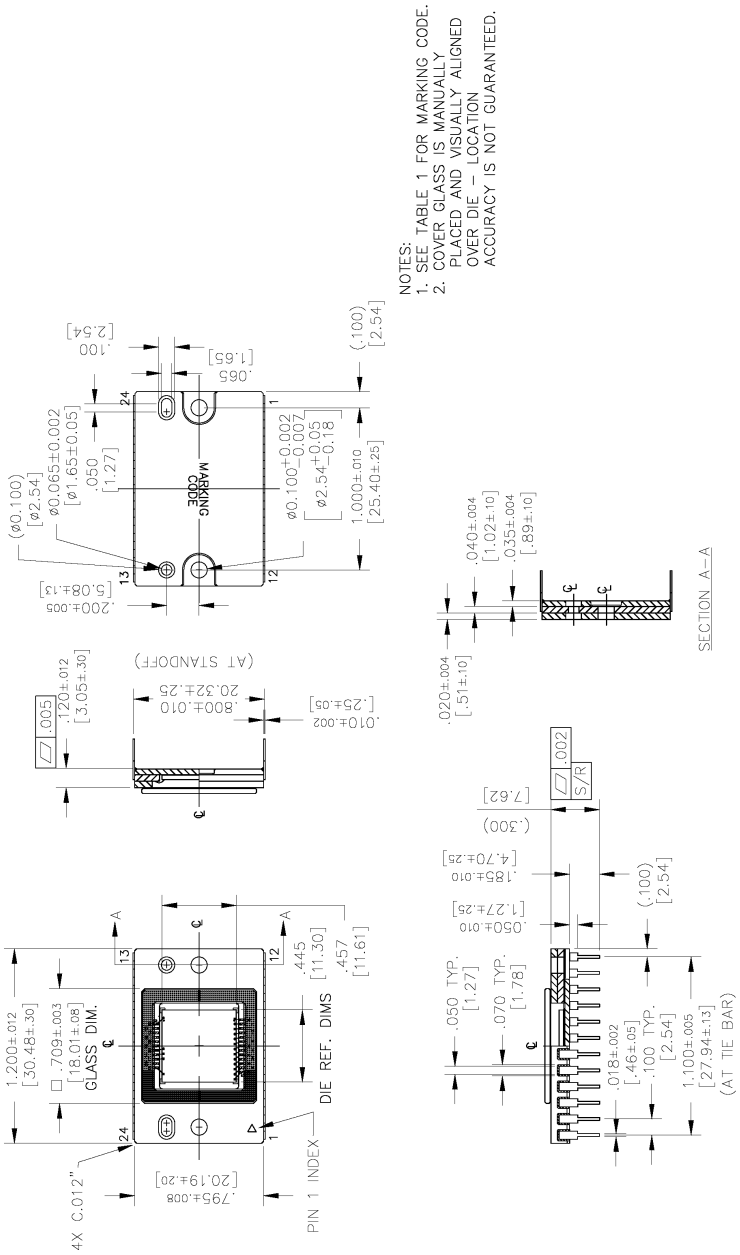

Figure 6: Completed Assembly (1 of 2)

NOTES:
1. CENTER OF IMAGE IS OFFSET FROM CENTER OF PACKAGE BY (.05, .00)mm NOMINAL.
2. DIE IS ALIGNED WITHIN +/- 2 DEGREE OF ANY PACKAGE CAVITY EDGE.

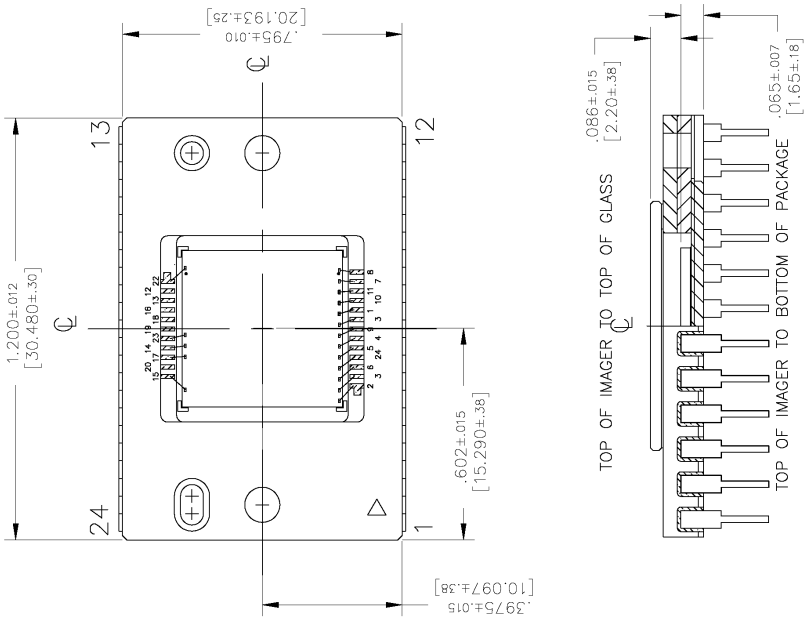

Figure 7: Completed Assembly (2 of 2)

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

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REVISION CHANGES

Revision Number	Description of Changes
1.0	Corrected Figure 4, Pinout Diagram. Updated DC Operating Conditions, Section 2.4. Updated CCD Parameters Specific to Low Gain (high dynamic range) Output Amplifier (page 13)
2.0	Corrected Figure 4, Pinout Diagram. (Pixel locations incorrect.) Updated DC Operating Conditions for Output Gate (Section 2.4). Updated CCD parameters Specific to Low Gain (High Dynamic Range) Output Amplifier for Dynamic Range (page 13). Removed appendix.
3.0	First version of the document in S9K. Formerly Revision 2 in hard copy format. Removed Class 0 from the Cosmetic Specification and UV coated device. (Section 3.2) Added ESD classification. (Section 2.3) Replaced Quality and Reliability notes with current format. (Section 4.2)
4.0	Update specification format Updated Completed Assembly Drawing

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