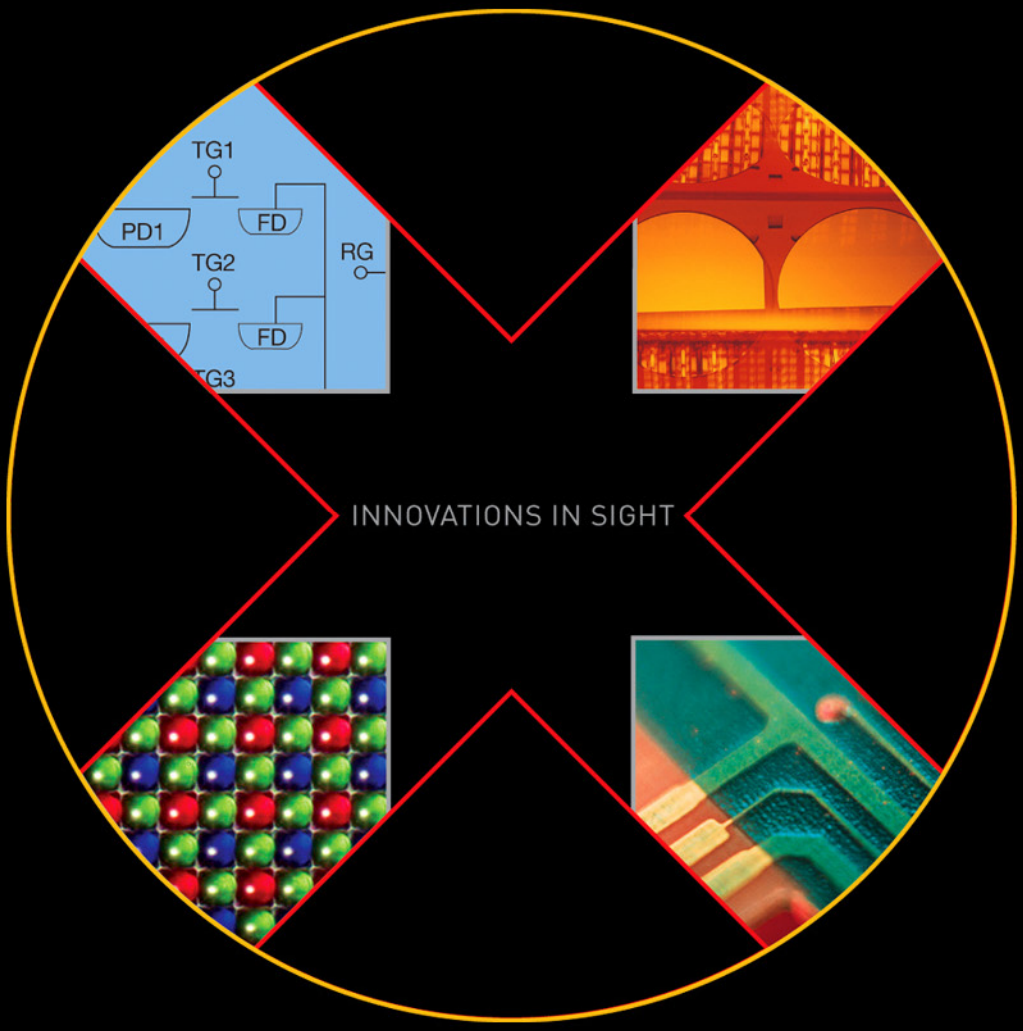
USERS MANUAL

Revision 8.0 MTD/PS-0215

January 2, 2008



KODAK KAF SERIES CCD DIGITAL REFERENCE

EVALUATION BOARD USERS MANUAL

Kodak

Image Sensor Solutions

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INTRODUCTION

The Kodak *Digital Science* ™ KAF Series CCD Digital Reference Evaluation Board provides a powerful platform to quickly and easily implement a Kodak Digital Science Full Frame or Blue Plus Full Frame CCD image sensor in a prototype imaging system.

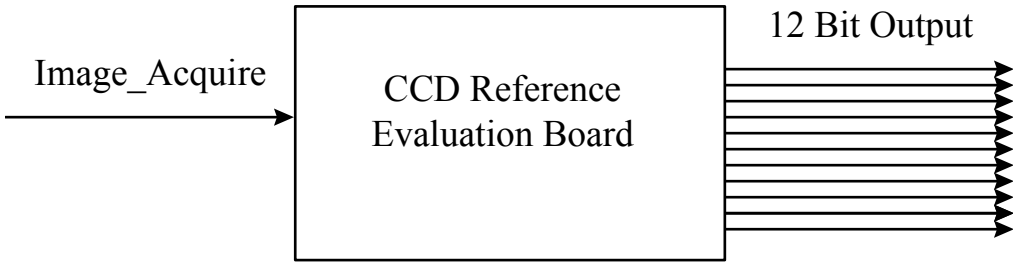
The Evaluation Board also serves as a useful reference design that will save considerable time and cost in the development of a product prototype. The programmable logic architecture, bias supplies, clock drivers and analog signal processing chain can be readily used, with application specific modifications, in a camera production design.

The Evaluation Board is designed to be flexible, and has the ability to operate many different Kodak Full Frame image sensors at different operating frequencies. Consult Image Sensor Solutions (ISS) to obtain information for optimizing the reference design to operate a specific image sensor at a specific operating frequency.

OVERVIEW

The KAF Series Digital Reference Evaluation Board serves as a complete, self-contained, CCD image acquisition sub-system. The user simply applies power, and an IMAGE_AQUIRE TTL pulse to begin capturing digital images. Differential TTL frame grabber sync pulses (Frame, Pixel and Line rate) are provided to facilitate easy connection to a frame grabber.

In the still capture mode, application of the IMAGE_ACQUIRE signal results in flushing of the CCD, then integration, then clocking out of a full frame of image data. In free-run mode, an acquisition signal is not needed; the board is free running and continuous frames of 12 bit information stream out.



SPECIFICATIONS

Maximum Data Rate	6MHz
Resolution	12 Bits
Frame Rate	Depends on Data Rate, CCD Array size, and Integration time.

OUTPUTS:

D[11..0]	Differential TTL
Frame Grabber Syncs	Differential TTL
Integration Sync	TTL

INPUTS: TTL

Serial Clock	10 MHz Maximum

PGA Gain Range	1X to 6X
PGA Gain Resolution	256 steps
Offset Range	-100mV to +100mV
Offset Resolution	256 steps

Temperature Range Board	0 - 70°C
Temperature Range CCD	-50 to +70°C typical

Power Supplies				Typical Current Switching Power Supply	
Supply	Minimum	Nominal	Maximum	Disabled	Enabled
+5V	+4.9V	+5V	+5.1V	1000mA	1500mA
+18V	+17V	+18V	+20V	120mA	-
-18V	-20V	-18V	-13V	100mA	-

Electrons per A/D count	29.2 @ 5MHz, 2.5X Gain setting (Assuming on-chip CCD amplifier gain CCD of 10μV/electron)
RMS Dark Noise	1.9 LSB typical @ 5MHz, 2.5X Gain setting
System Noise Floor	56 electrons @ 5MHz, 2.5X Gain setting (Assuming on-chip CCD amplifier gain of 10μV/electron)

ARCHITECTURE OVERVIEW

A complete Block Diagram of the CCD Digital Reference Evaluation Board is shown in .

MASTER CLOCK

The Master Clock runs at eight times the Pixel clock frequency. The maximum pixel clock frequency is 6 MHz, which yields a maximum system clock frequency of 48 MHz. For slower Pixel clock frequencies, decrease the master clock frequency. The Default setting of the evaluation board is a 40 MHz system clock, with a pixel clock frequency of 5 MHz.

The KAF-4301E is an exception to this. It provides pixel frequencies of 2.5MHz and 1.25 MHz by dividing the 40MHz master clock by 16 and 32. The pixel frequency is selected using SW2. This is an 8-position switch that usually selects a CCD binning mode (see section Binning Modes). The KAF-4301E timing program does not support binning at this time and, instead, uses this switch to select the pixel rate (see Table 5: KAF-4301E SW2 Pixel Rate Settings). The pixel rate is 1.25 MHz when SW2 is set to position 0 and 2.5 MHz when set in any other position.

PLD1

PLD1 contains the Clocking State Machine that controls the operational flow of the evaluation board (Figure 2: Clocking State Machine). PLD1 generates the CCD clock timing, A/D converter timing and frame grabber sync signals. The PLD1 controls the image line and frame length [dependent upon the CCD switch settings], as well as the horizontal and vertical CCD clock timing [dependent upon the binning mode BIN switch settings.]

PLD2

PLD2 controls the integration timing, which is dependent upon the INT switch settings. PLD2 also programs the AD9816's registers to a default condition upon power up via a three wire serial interface. Additionally, if the user chooses to adjust the AD9816's register settings, the PLD2 controls the programming of these registers.

CCD CLOCK DRIVERS

Elantec clock drivers, designed to drive the large capacitance loads presented by the clock gates of the CCD, are used to generate the horizontal and vertical clocks. The Elantec drivers accept TTL inputs, and level shift to the required peak-to-peak voltage swing of the CCD clocks. The peak-to-peak swing of the clocks is adjustable. The outputs of the drivers are AC coupled, providing adjustable offset of the clocks from the negative rail to the positive rail. Using a separate IC for each vertical clock (V1,V2), a maximum 4 amp output drive current per vertical clock channel is available. A single IC is used to drive H1, and H2, giving a maximum 2A output drive current per Horizontal clock channel.

The reset clock driver utilizes two fast switching transistors, designed for a fast switching input signal with a narrow pulse width. The peak-to-peak voltage swing and the offset voltage are adjustable.

CCD BIAS VOLTAGES

CCD bias voltages (VRD, VOG, VLG) are supplied by filtered outputs of adjustable potentiometers. Fixed CCD bias voltages (LOD, VSS, GUARD) are supplied by filtered outputs of voltage dividers.

CCD IMAGE SENSOR

This evaluation board supports the following Kodak Full Frame (KAF) CCD image sensors:

KAF-0261E, KAF-0402E, KAF-0402ME, KAF-0401LE, KAF-1001E, KAF-1301E, KAF-1301LE, KAF-1402E, KAF-1402ME, KAF-1602E, KAF-1602LE, KAF-3200E, KAF-3200ME, KAF-4202, KAF-6303E, KAF-6302LE, KAF-16801E, KAF-16801LE, KAF-4301E

A/D CONVERTER: ANALOG DEVICES AD9816

The AD9816 is a 12 bit, 6 MSPS CCD analog signal processor. The IC provides an integrated correlated double sampling (CDS), 8 bit programmable gain, and 8 bit DC offset adjust. Timing signals are provided by PLD1. Default register values are downloaded from PLD2 upon power up. Alternate programming of its registers can be achieved via external serial interface or by manually setting the address and data switches on the board and pressing the capture button.

EMITTER FOLLOWER

The video out of the CCD is buffered using a bipolar junction transistor in the emitter follower configuration.

AC COUPLING CAPACITOR

A 1200pF input coupling capacitor removes the DC component of the video signal.

POWER ON CLEAR / RESET

Resets and initializes the board on power up or when the Reset button in pressed.

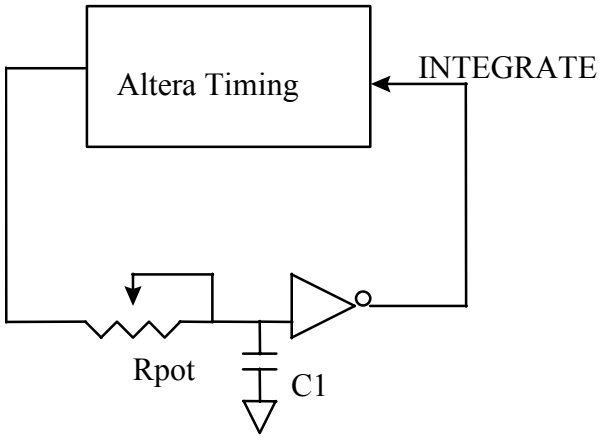
JTAG HEADER

A 10-pin header provides the user with the ability to reprogram the Altera 7000S PLDs in system via Altera's ByteBlaster programming hardware.

UNIT INTEGRATION TIME

Integration Timing:

The amount of time the CCD is exposed to light before clocking out the accumulated charge is called the integration time. An RC circuit and Schmitt trigger inverter are used to set the unit integration time. Total integration time is a multiple of the unit integration time.



Set Unit Integration

The circuit is set to toggle at 100 Hz, providing a fixed unit integration time of 10ms. The actual integration time is set to a multiple of the unit integration time using an internal integration counter in PLD2. The user can choose an integration time from 10ms to 10 seconds by setting the integration switches appropriately (see Table 6: Integration Time Modes)

J6 INPUT CONNECTOR

This connector is used to input control signals to the evaluation board. This is an optional feature; all control lines can be set via on-board switches. Images can be acquired using the on-board image capture button. No external digital inputs are needed to acquire images.

J4 OUTPUT CONNECTOR

The J4 output connector provides 12 bits of video data in RS422 differential TTL format. J4, additionally, provides three frame grabber sync signals in differential TTL format.

J7 INTEGRATION SYNC

This connector provides a sync signal that is high during the integration time period. The signal can be used to sync a shutter or LED light source to the evaluation board, and can source up to 80mA at 5V.

J1, J2 IMAGER BOARD CONNECTORS

CCD Daughter Boards plug into these connectors. The daughter boards route the clock and bias traces from the timing board to the proper pins of the CCD.

POWER SUPPLIES

An onboard switching supply provides all of the voltages necessary to operate the CCD Digital Reference Evaluation Board, from a single +5V source.

Switching supplies can, however, be a source of low-level asynchronous noise. If asynchronous noise is present and objectionable in an application, the internal switching supply can be disabled and external low-noise linear supplies can be used to power the board. The procedure for configuring the board to accept external supplies is detailed Under Power Supply Modes

J5 POWER CONNECTOR

The power connector is a 5-pin connector with +5V, +18V, -18V and two AGND connections. If the switching power supply is used to generate the +15 and -10V supplies, then only an external +5V supply needs to be brought in through J5. Otherwise, all three power supplies must be connected to the board via J5.

BOARD REQUIREMENTS:

POWER SUPPLY

The board requires only a single +5V, 1.5 Amp or greater power supply to operate. An on board switching power supply generates the necessary +15V, 120mA and –10V, 120mA power supplies from the 5V input. Although extensive filtering is done on board, the power supplied to the board must be quiet and stable in order to achieve the best possible performance.
(See Power Supply Modes, for an alternative way to power the board.)

INPUTS

In the Free-Run mode, the evaluation board requires no input signals to begin acquiring images.

In Still mode, the evaluation board will acquire a single image on the falling edge of the Image_Acquire control line. This can be accomplished via the push button (S4) or, remotely, by utilizing the Image_Acquire control line.

See Section Still/Free-Run Modes for more information on Still and Free-Run modes.
See Sections Line/Switches Modes and section AD_IN/EX Modes for information on additional optional inputs.

OUTPUTS

D[11..0] (+/-)	12 bits of Differential TTL Digital information
INTEGRATE	A signal provided to allow the user to synchronize the strobing of LED illuminators or opening of a shutter, during the integration period.
FRAME (+/-)*	Differential TTL Frame grabber vertical sync signal.
LINE (+/-)*	Differential TTL Frame grabber horizontal sync signal.
PIX (+/-)*	Differential TTL Frame grabber pixel sync

Note: These sync signals can be modified if necessary to accommodate different Frame Grabbers.

JTAG PROGRAMMING

Altera 7000S In System Programmable (ISP) PLD's are used on this board. A ten-pin header (J8) is provided to allow for the programming of these PLD's. Since these parts are re-programmable, custom digital logic can be implemented for timing and mode adjustments or additions. Any custom implementation can be made quickly and easily to via the JTAG programming interface provided by this connector.

CONFIGURATION MODES

The following modes of operation are available to the user:

LINE/SWITCHES MODES

The Line/Switches Jumper (SW5) Selects whether some of the board settings will be controlled externally through the J6 connector (Line), or via the on-board switches (Switches). If this switch is set to Line, then the integration time and the binning mode must be set remotely via digital I/O. The still/free-run mode switch (SW3, 3-position switch) can also be set externally when the Line mode is selected. Set SW3 to the middle position if it is desired to control this line externally.

STILL/FREE-RUN MODES

The "Still/Free-Run" switch (SW3) is a three-position switch that selects whether the board will operate in the still mode, or a free-running mode.

If SW3 is placed in the middle position ("LINE"), the image capture mode is determined by the voltage on the STILL/FREE-RUN pin on the input connector (J6-27). Setting this line LOW selects the free-run mode, and setting it HIGH selects the still mode.

In still mode, the Image_Acquire control line must be strobed in order to acquire a single image. This is accomplished by either pressing the on-board acquire button (S4) or, remotely, by bringing the Image_Acquire line low and then back high. The detection of the falling edge of this signal starts the image acquisition process.

The still mode acquisition process is as follows:

1. The CCD is flushed of all accumulated charge.
2. The CCD is exposed to light during the integration time.
3. The image is clocked out of the CCD. The system then waits for the next Image_Acquire signal.

In the Free-Run mode, the system will continuously capture images and clock them out. No flushing is done, as the clocking out of the previous image serves this same purpose.

See Figure 2: Clocking State Machine for the Clocking State Machine Diagram.

AD_IN/EX MODES

The board comes with an Analog Devices AD9816 12 bit A/D converter on board. This A/D has several features, such as multiple configurations, programmable gain, and offset registers which require initialization and/or programming on power up. The programming of these registers is done via a three wire serial interface.

EXT:

A three wire serial interface is provided on the J6 connector of the board, and the AD9816 registers can be controlled remotely via these when the A/D_IN/EX Jumper (SW4) is set to EXT. See Figure 3: AD9816 Register Configuration for AD9816 serial timing diagrams and information.

INT:

If it is not desired to control the programming of the A/D's registers remotely, set Jumper SW4 to INT. PLD2 contains a state machine that serially loads in the following default values to these registers upon power up.

A/D Default Register Settings:

No. of channels:	1
Mode:	CDS Mode
Input Span:	3V
Channel Selected:	Green
Red PGA Gain*:	1
Green PGA Gain:	1
Blue PGA Gain*:	1
Red Offset*:	0mv
Green Offset:	0mv
Blue Offset*:	0mv

Note: Although the Red and Blue channels are not used, these registers are still initialized to these default settings

ADJUSTMENTS

Adjustments can be made to the A/D registers during operation of the board by utilizing the DATA dipswitch (SW10), the ADDRESS switch (SW9), and the Image_Acquire control line. After setting SW9 to the desired Address, and SW10 to the desired Data, send an Image_Acquire signal either by pressing the Image_Acquire button or remotely via the J6 connector control line. This will load the new value into PLD2 and a state machine inside the PLD will then serial load the new data into the A/D's register. This is true whether or not the board is running in Still or Free Run Mode. (See Figure 3: AD9816 Register Configuration for more information on the AD9816 registers.)

CCD MODES

The CCD Select switch (SW1) setting determines the line and frame length timing.

This switch is pre-set at the ISS. (See Table 2: CCD Modes)

BINNING MODES

The BIN Select switch (SW2) setting determines the Binning mode operation. (Table 3: Binning Modes)

INTEGRATION MODES

The INT Select switches (SW6, SW7) settings determine the Integration Time.

SW6 is the Coarse Adjust. SW7 is the Fine Adjust. (Table 6: Integration Time Modes)

FRAME GRABBER DIAGNOSTIC MODES

When set to ENABLE, the Sync_Test_Enable switch (SW12) tri-states the 12-bit output bus out of the A/D converter, and enables the output of either the pixel number or the line number onto the output bus, depending on how the Sync_Test_pix/line Jumper is set (SW11). This provides a diagnostic test to make certain the Frame Grabber is synchronized correctly with the board.

The line counter in PLD1 is a binary up-counter, therefore the line count that is output to the output bus will increment sequentially (0,1,2,3,4,5.....) until the last line in the frame.

The pixel counter in PLD1 is a gray code up counter, therefore the pixel count that is output to the output bus will increment in gray code transition counts (0,1,3,2,6,7,5,4.....) until the last pixel in the line.

POWER SUPPLY MODES

Power can be supplied to the board in one of two ways:

Switching Power Supply

The board comes supplied with a 500 kHz switching power supply (Linear Technologies LT1372). If it is desired to utilize the on-board switching supply, the board should be configured as follows:

1. Connect a 5V, 1.5A or greater lab supply to the J5 power connector.
2. Install Jumper 6 and Jumper 4.
3. Remove Jumper 7 and Jumper 5.
4. Set Jumper 1 to the ON position.

External Supply Operation

To disable the on-board switching supply and operate using external supplies:

1. Remove Jumpers 4 and 6;
2. Install Jumpers 5 and 7;
3. Move Jumper 1 to the "OFF" position to disable the switching power supply;
4. Connect +18V, -18V, and +5V to power input connector J5.

Functionality

The switching supply generates +15V and –10V supply "islands". The same is true for the +15V and –10 V regulators on the board. Jumpers 4 and 6 connect the switcher supplies to the +15V, -10V power plane. Jumpers 5 and 7 connect the regulated outputs to the +15V, -10V power plane. Jumper 1 either enables or disables the LT1372 Switcher.

CCD IMAGER BOARDS

Each CCD has an imager board. The imager boards route the bias voltage traces from the timing board through connectors J1 and J2 to the appropriate pins on the device. The imager boards contain the Horizontal and Reset clock driver ICs as well as the emitter-follower circuit that buffers and drives the video signal down to the timing board.

ADJUSTMENTS

Fixed Bias Voltages:

Fixed Voltages:

VDD	+15V
LOD/GUARD	+10V
VSUB	0V
VSS	0 to +2.1V*

Note: The VSS bias voltage is set by the inclusion of up to three series diodes on the imager board. Therefore 0V is achieved by shorting across all three diode positions. This bias is preset at the factory depending on the appropriate CCD specification.

Variable Bias Voltages:

Variable Voltage:*	Function	Adjustment Potentiometer
VOG		R12
VRD		R11
VLG		R13
V_PP	(vertical clk peak to peak swing)	R17
VCLK	(vertical clk level adjust)	R67
H_PP	(horizontal clk peak to peak swing)	R64 (imager board)
HCLK	(horizontal clk level adjust)	R14 (imager board)
R_PP	(reset clk peak to peak swing)	R18 (imager board)
RCLK	(reset clk level adjust)	R27 (imager board)

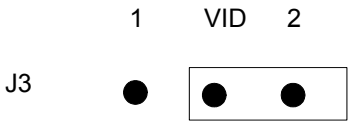
Note: These voltages are optimized for the particular KAF Series image sensor being used and are fixed at the factory according to the image sensor specification. Adjustments should not be made to them without consulting the ISS.

OUTPUT SELECTION FOR SENSORS WITH TWO OUTPUTS

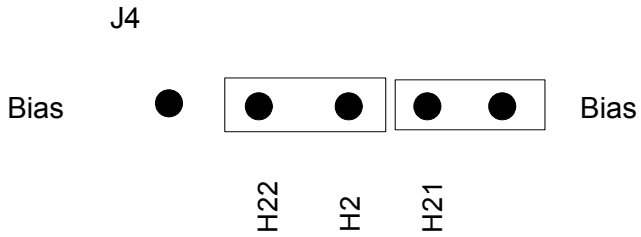
The KAF-1001E, KAF-0261E, and KAF-4301E sensors have two video outputs. The outputs have different gain and one of them is selected depending on the application. The imager daughter boards for these sensors have two jumpers that must be set correctly to enable the desired output.

To select the high gain output, Vout2:

Set J3 to the VID2 position:

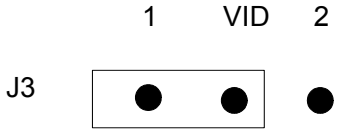


Set the two jumpers on J4 as follows:

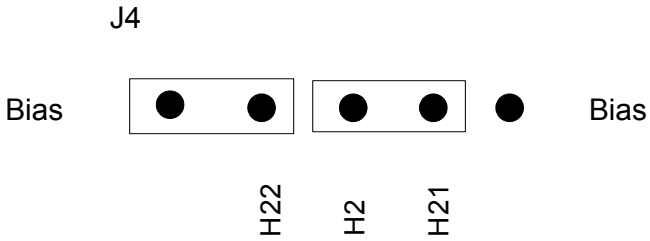


To select the low gain output, Vout1:

Set J3 to the VID1 position:



Set the two jumpers on J4 as follows:



Note: The schematic for the KAF-1001 imager daughter board contains an error. The library element for the imager indicates that pin 5 is Vout1 and pin 12 is Vout2. These are incorrect and are reversed in that part of the schematic. However, the labeling on the imager board is correct. Only the pin labeling on the schematic is incorrect.

TIMING

FIXED TIMING:

H1, H2

VARIABLE TIMING:

V1, V2 (binning modes)

RESET (binning modes)

CLAMP (binning modes)

SAMPLE (binning modes)

A/D Clock (binning modes)

See Timing Diagram 1 – Figure 4: Pixel Rate Timing

See Timing Diagram 3 -Figure 12: Binning Mode Timing (2x2 binning shown)

Note: Not available with the KAF-16801E, KAF-16801LE and KAF-4301E image sensors.

OTHER PARAMETERS

FIXED PARAMETERS:

Flush Duration: (4000 lines)

VARIABLE PARAMETERS:

Pixel frequency: The pixel frequency is 1/8 the master clock. The maximum pixel frequency is 6MHz. To run the board at a slower pixel rate, decrease the system clock frequency, keeping in mind the 1/8 relationship. (e.g. for a 4 MHz pixel rate, use a 32 MHz system clock)

Line length (Depends on CCD mode)

Frame length (Depends on CCD mode)

Vwidth (Depends on pixel frequency, 64 pixel counts wide)

Unit Integration:The integration clock frequency is set by a RC circuit of R6 and C6 and is adjusted to 100Hz at the factory, creating a unit integration time of 10ms. By adjusting R6, the unit integration time can be varied. Because all of the integration time settings in Table 6: Integration Time Modes are multiples of this unit integration time, the values would need to be recalculated for any new unit integration time.

FIGURES, TABLES, TIMING DIAGRAMS, AND PERFORMANCE DATA

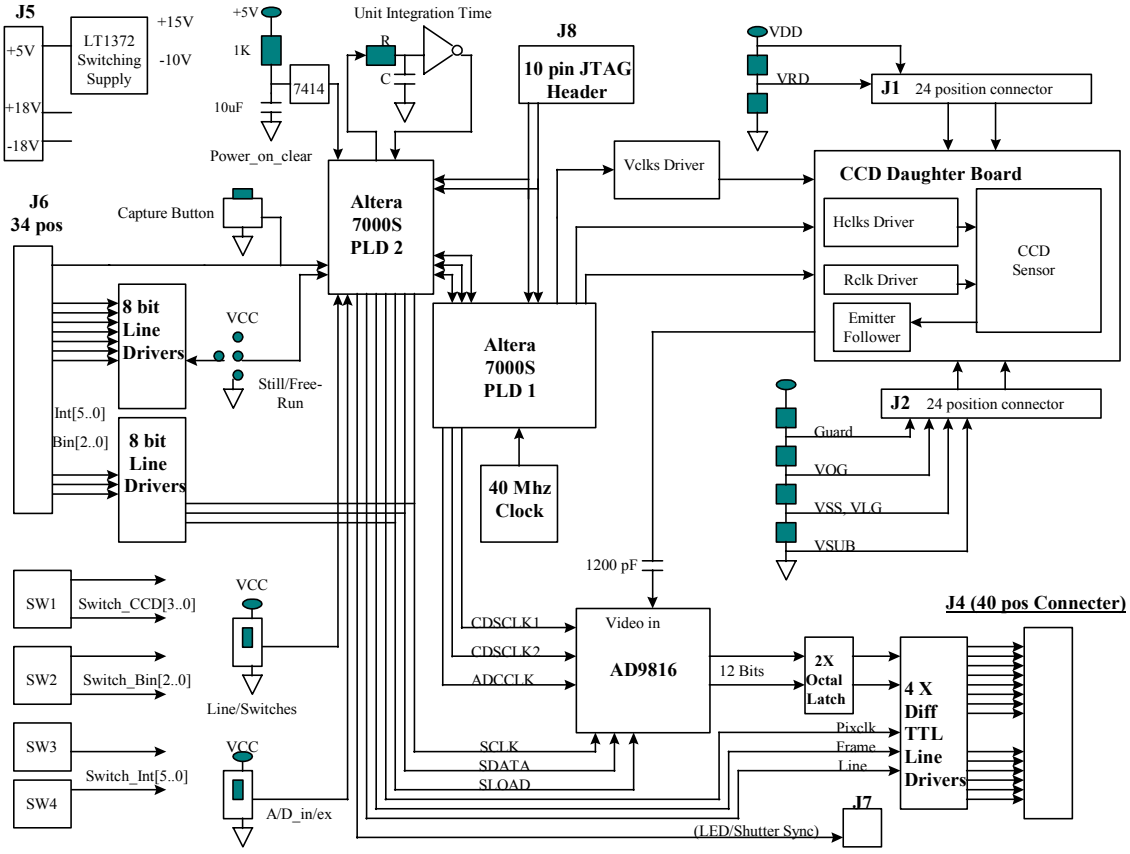


Figure 1: System Block Diagram

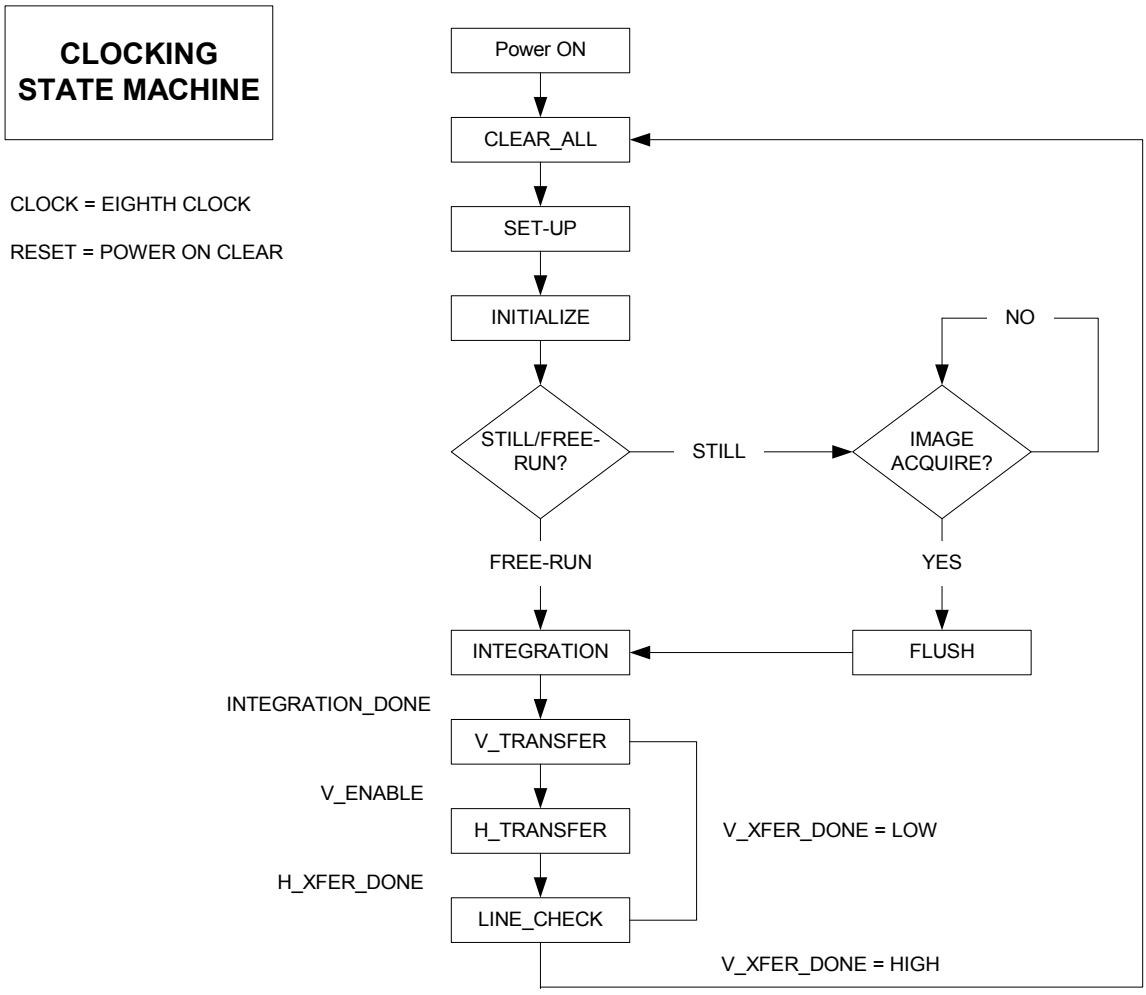
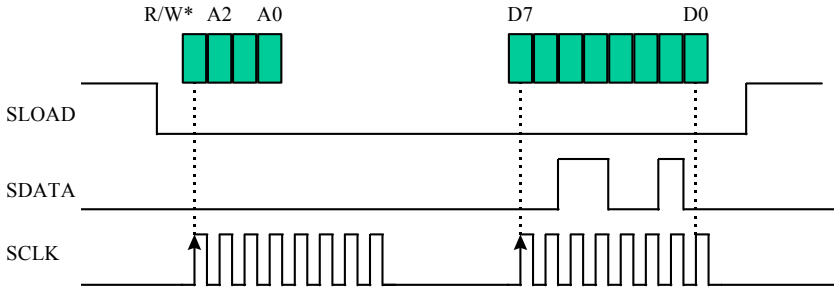


Figure 2: Clocking State Machine

Address	Register		Function	Default Programming
0	Configuration Register			
	bit 7 MSB	test mode bit	always 0	0
	bit 6	test mode bit	always 0	0
	bit 5	CDS mode bit	High for CDS Low for SHA mode	1
	bit 4	input span	High for 3V	1
	bit 3	input span	High for 1.5V	0
	bit 2	channel mode	High for 3 channel	0
	bit 1	channel mode	High for I channel	1
	bit 0	test mode bit	Always 0	0
1	MUX Register			
	bit 7	test mode bit	always 0	0
	bit 6	channel sequence	High for BGR	0
	bit 5	channel sequence	High for RGB	0
	bit 4	channel select	High for Red	0
	bit 3	channel select	High for Green	1
	bit 2	channel select	High for Blue	0
	bit 1	test mode bit	always 0	0
	bit 0	test mode bit	always 1	1
2	Red PGA Register		1X to 6X*	0 (1X)
3	Green PGA Register		1X to 6X*	0 (1X)
4	Blue PGA Register		1X to 6X*	0 (1X)
5	Red Offset Register		-100mv to 100mv**	0 (0mV)
6	Green Offset Register		-100mv to 100mv**	0 (0mV)
7	Blue Offset Register		-100mv to 100mv**	0 (0mV)

Note: PGA Gain = 1+(gain code/ 51.2) ** 01111111 = +100mV, 00000000 = 0 mV, 11111111 = -100mV



3 Wire Serial Interface Timing

* R/W Low for Write, High for Read

Figure 3: AD9816 Register Configuration

Switches	Line/Switches	Select where control of modes comes from
	Switch_Int[5..0]	Integration timing control lines
	Switch_Bin[2..0]	Binning mode control lines
	Switch_CCD[3..0]	Device Select (KAF 0400, KAF1600 ...)
	Still/Free-Run	Selects mode of operation
	A/D_in/ex	Select how A/D programming is controlled
	Sync_test_pix/line	Select frame grabber diagnostic to be performed
	Sync_test_enable	Enable/Disable frame grabber sync test

Inputs	System_clk	8X Pixel clock (48 MHz maximum)
	integrate_clk	Unit Integration Time clock
	Image_Acquire	Still mode image acquisition command line, OR, Capture button input
	Int[5..0]	Integration timing control lines
	Bin[2..0]	Binning mode control lines
	Serial Clock	For A/D use
	Serial Data	For A/D use
	Serial Load	For A/D use
	JTAG Header	10-pin header for ISP

Outputs	Dout[11..0](+/-)	12 Bits Differential TTL Digital information
	FRAME (+/-)	Differential TTL frame grabber frame sync signal
	LINE (+/-)	Differential TTL frame grabber line sync signal
	PIX (+/-)	Differential TTL frame grabber pixel sync signal
	INTEGRATE	Active high signal indicates when in integration state. Can be used to sync LED's or shutter with this state.

Table 1: Board Inputs, Outputs, Switches

CCD Switch Setting	CCD	Pixels/Line	Lines/Frame
0*	Test Mode1 or KAF-16801E/LE	100	2
1	KAF-1401E	1500	1200
2	Test Mode 2	10	4
3	KAF-1301E, KAF-1301LE	1500	1200
4	KAF-4202	2300	2150
5	KAF-1602E, KAF-1602LE	1700	1100
6	KAF-6303E, KAF-6302LE	3300	2150
7	KAF-0401E, KAF-0401LE	1000	650
8	KAF-3200ME	2300	1600
9	KAF-1001E	1200	1150
A	KAF-0261E	700	650
B	KAF-16800	4300	4200
C	KAF-4301E	2300	2200

Table 2: CCD Modes

Note: In order to operate the KAF-16801E/LE sensor using the KAF Series CCD Digital Reference Evaluation Board, the board is configured with a unique PLD program. This is the switch setting for the KAF-16801E and KAF-16801LE for that case. When the board is configured for the KAF-16801E/LE, this mode will produce 4300 pixels per line and 4200 lines per frame. For all the other sensors, this is a test mode as described in the table.

Bin Switch Setting	Binning Mode
1	1x1 (No Binning)
2	2x2
3	3x3
4	4x4
5	5x5
6	6x6
7	8x8
0	10x10

Table 3: Binning Modes

Note: Binning Mode is not included in the timing program for the KAF-16801E, KAF-16801LE and KAF-4301E image sensors.

Bin Switch (SW2) Setting	Binning Mode
1	1x1 (No Binning)
2	1x1 (No Binning)
3	1x1 (No Binning)
4	1x1 (No Binning)
5	1x1 (No Binning)
6	1x1 (No Binning)
7	1x1 (No Binning)
0	1x1 (No Binning)

Table 4: Binning Modes when Configured for use with the KAF-16801E/LE

Note: In order to operate the KAF-16801E/LE sensor using the KAF Series CCD Digital Reference Evaluation Board, the board is configured with a unique PLD program. That PLD program does not support binning modes other than 1x1 (normal full resolution readout).

KAF-4301E SW2 Setting	Pixel rate
0	1.25 MHz
1 .. 7	2.5 MHz

Table 5: KAF-4301E SW2 Pixel Rate Settings

SW7 Switch Setting (Coarse)	INT 5-3 Switch (Coarse)	Integration Time (Seconds)
0	000	0
1	001	1
2	010	2
3	011	3
4	100	4
5	101	5
6	110	7
7	111	9

SW6 Switch Setting (Fine)	INT 2-0 Switch Setting Fine	Integration Time (ms)
0	000	0*
1	001	20
2	010	50
3	011	100
4	100	200
5	101	300
6	110	500
7	111	800

Table 6: Integration Time Modes

Note: If both SW7 and SW6 are set to zero, the integration time is set to 10ms.

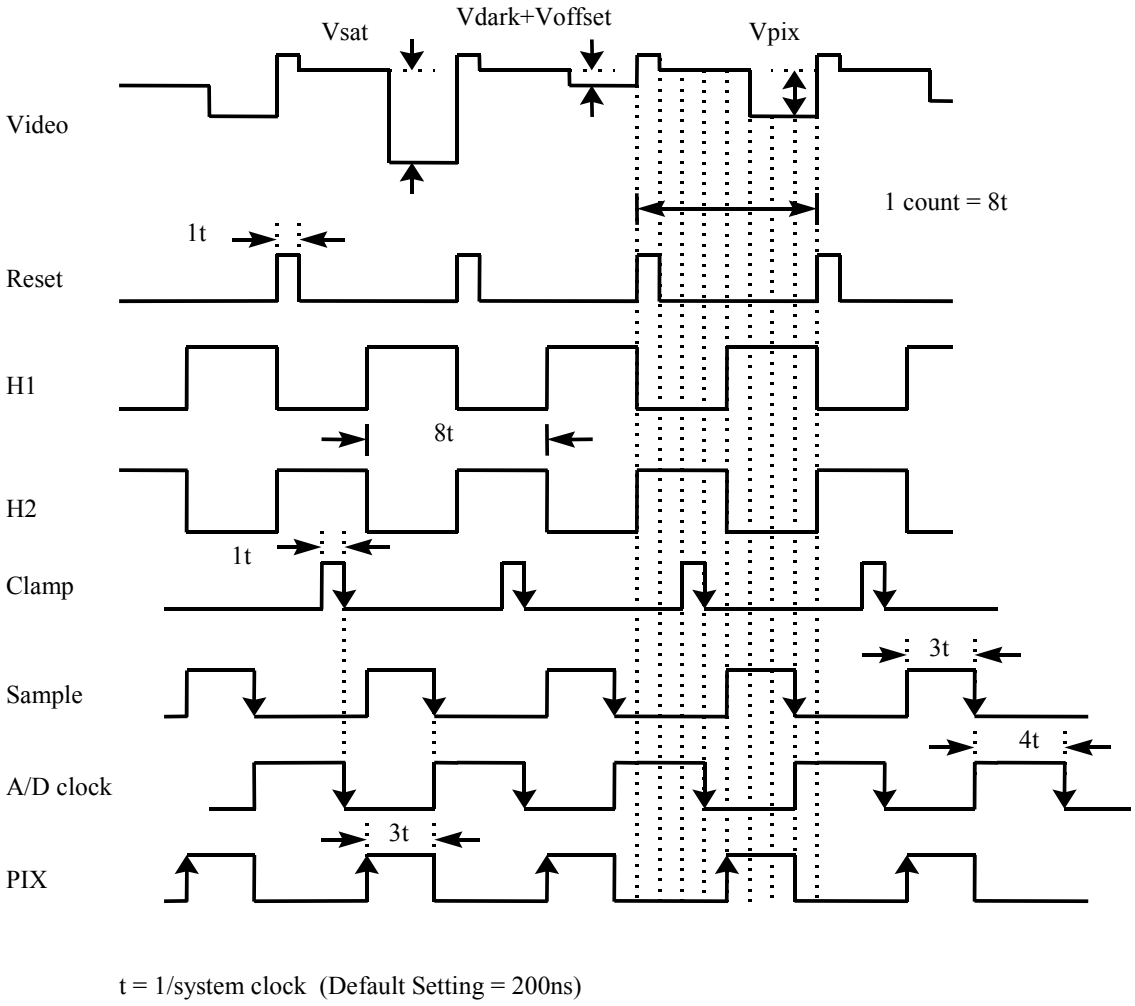


Figure 4: Pixel Rate Timing

Note: The KAF-4301E implements 16t = 1pixel and 32t = 1 pixel modes instead of the 8t=1pixel timing. This provides pixel frequencies of 2.5 MHz and 1.25 MHz.

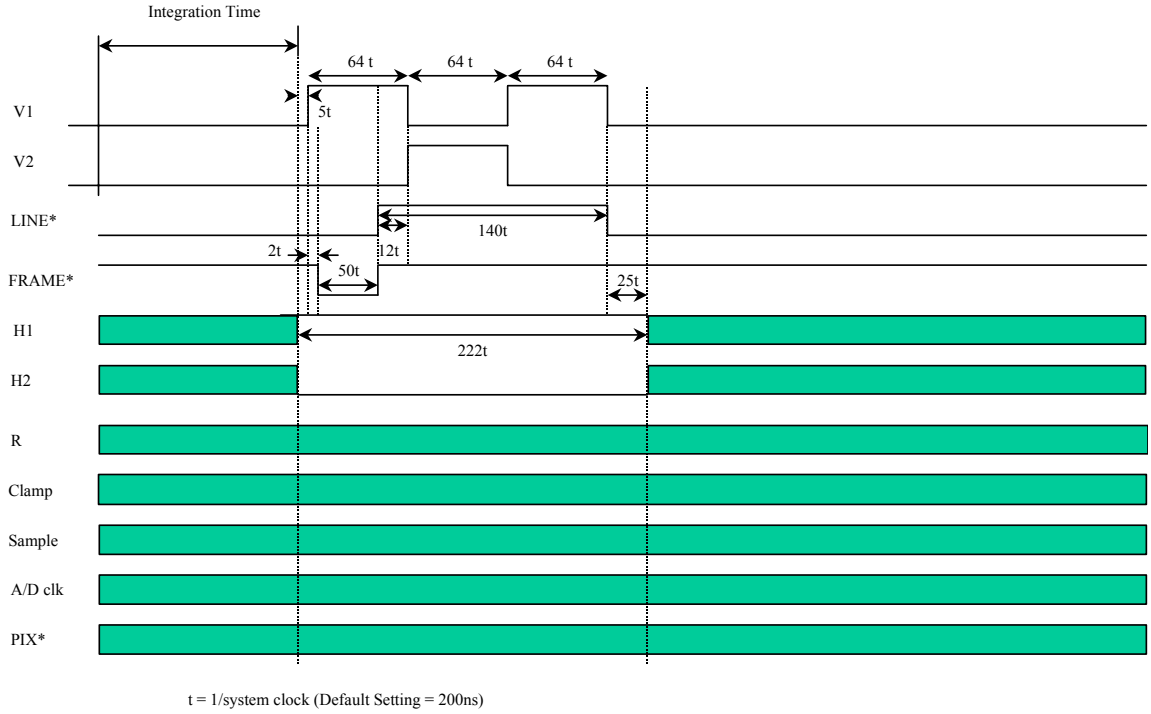


Figure 5: Line Rate Timing for KAF-0261E, 0402E, 1001E, 1301E, 1402E,

Note: The line rate timing for the KAF-4301E is similar to this with the addition of an overlap period in the vertical clock timing. Consult the current specification for the KAF-4301E for details.

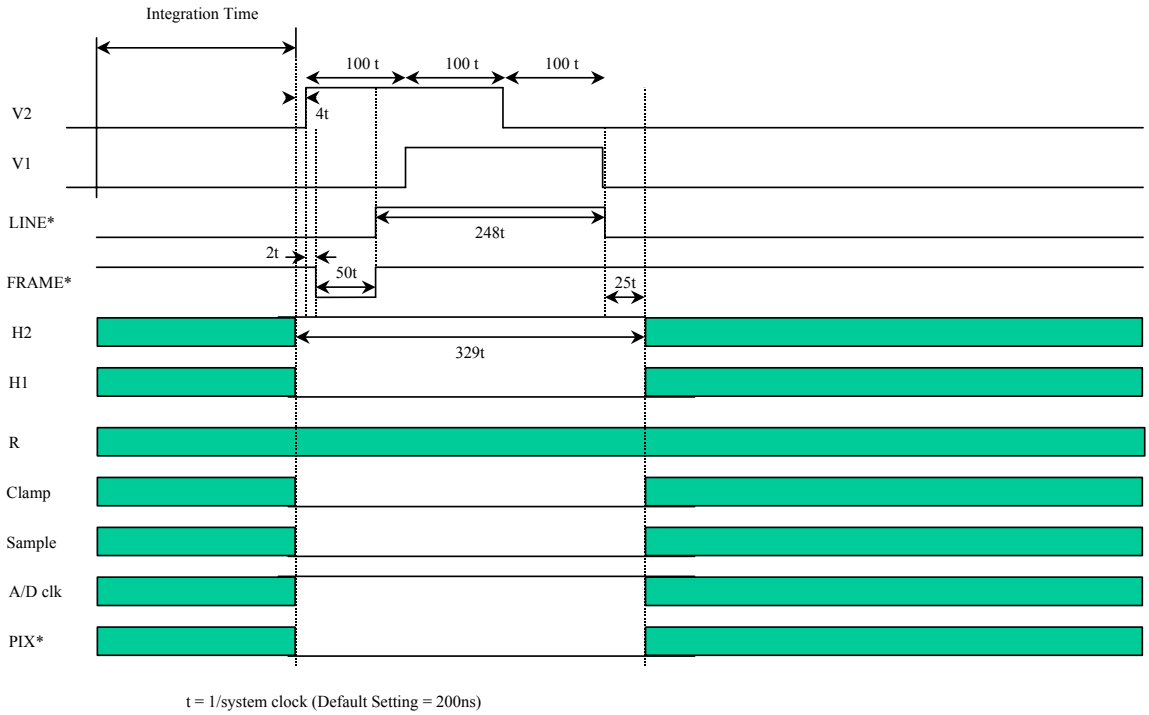


Figure 6: Line Rate Timing for KAF-16801E/LE Sensors

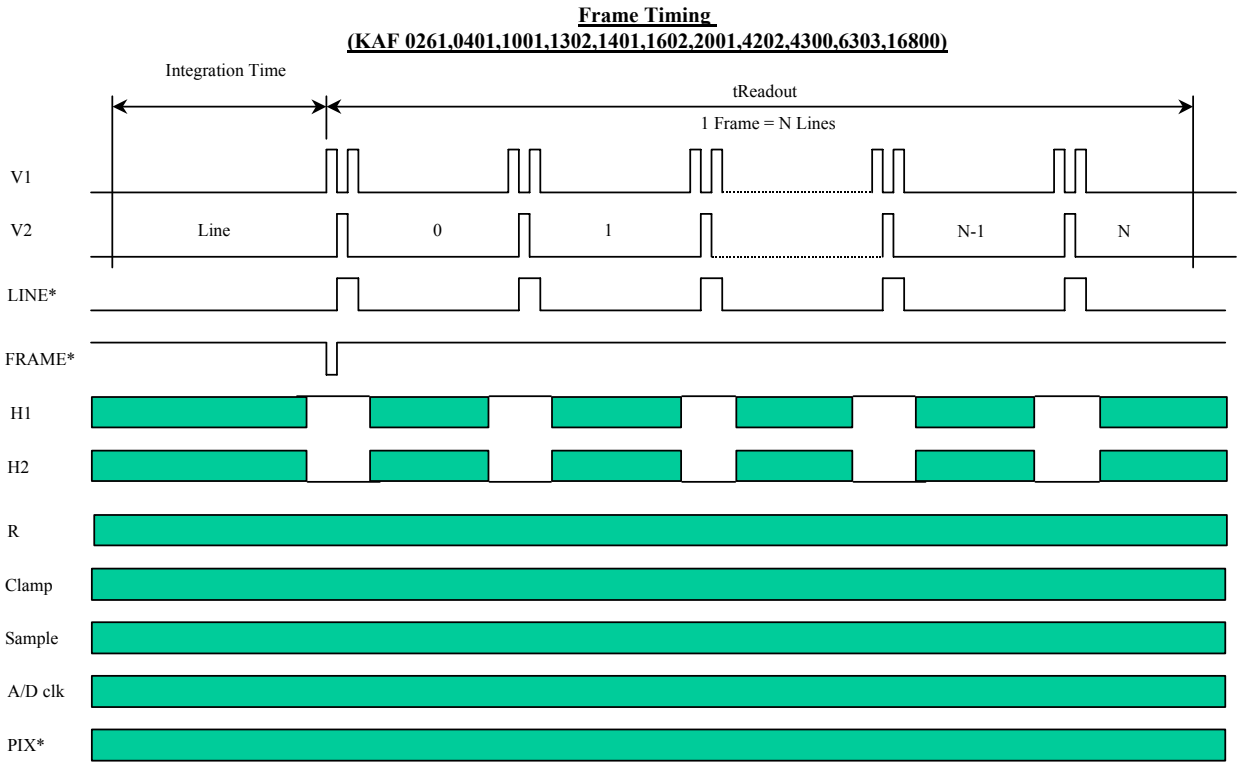


Figure 7: Frame rate timing for the KAF-0261E, 0402E, 1001E, 1301E, 1402E,

Note: Default Frame Grabber Settings

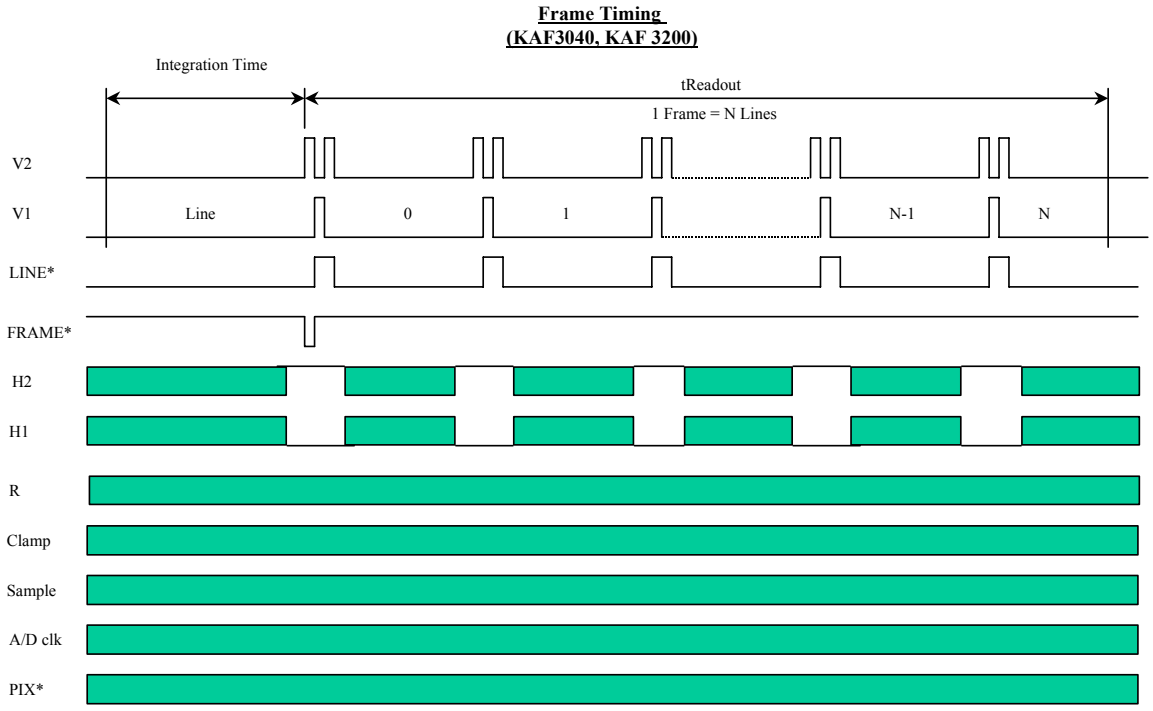
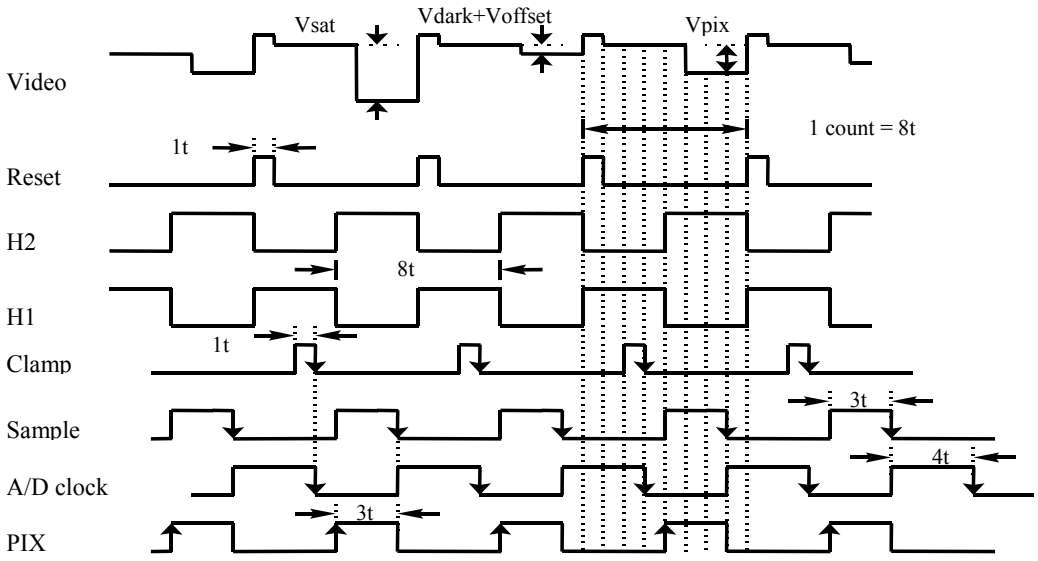


Figure 8: Frame Timing for the KAF-3200ME Sensor



t = 1/system clock (Default Setting = 200ns)

Figure 9: Pixel Rate Timing for the KAF-3200ME, KAF-16801E, KAF-16801LE Sensors

Still Mode: Flush and Integration Timing

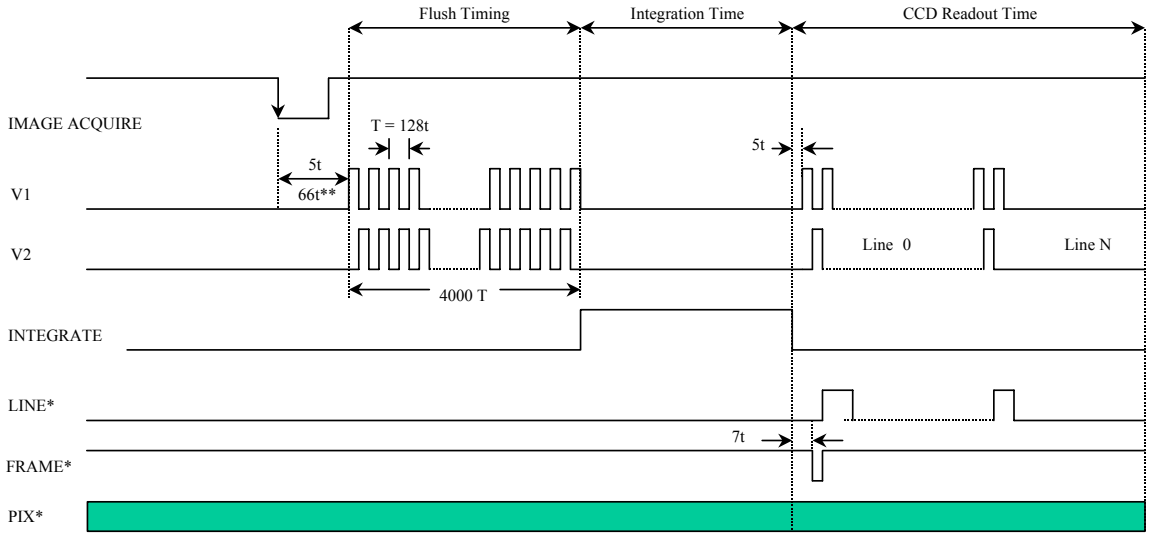


Figure 10: Still Mode: Flush and Integration Timing

Free Run Mode: Integration Timing

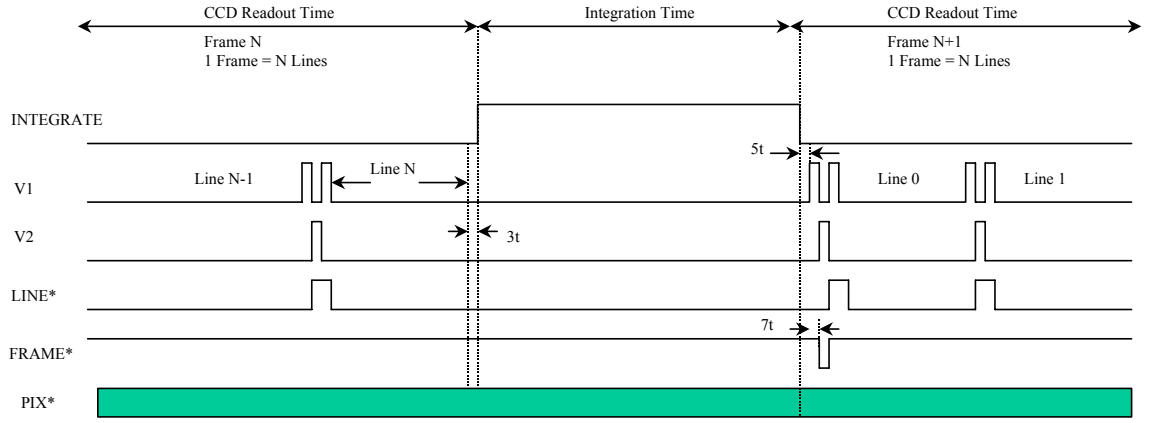
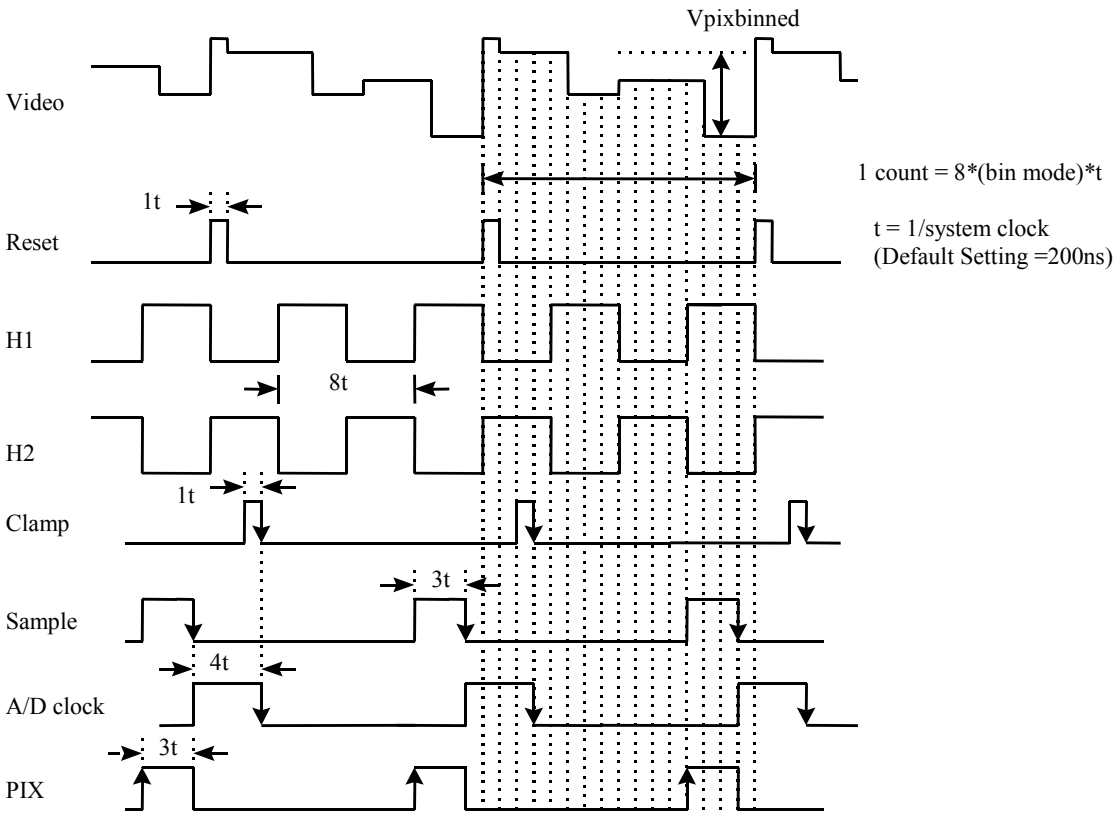


Figure 11: Free Run Mode: Integration Timing

t = 1/system clock (Default Setting = 200ns)

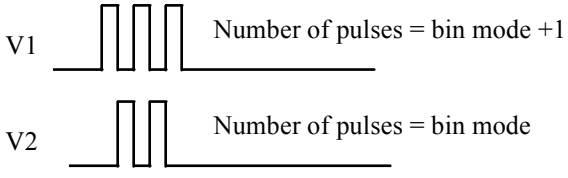
Note: Default Frame Grabber Settings



Pixel Rate Timing

Figure 12: Binning Mode Timing (2x2 binning shown)

In Binning Modes, the Frequency of the Reset, Clamp, Sample, A/D, and PIX clocks are decreased in order to allow charge to accumulate on the output node of the CCD before being reset. See Application Note MTD/PS-0900 KAF Series Full-Frame CCD Series Binning Mode Operation for more details on Full Frame CCD Binning.



Line Rate Timing

In Binning Modes, additional lines of charge are summed in the CCD's horizontal register before being clocked to the output node.

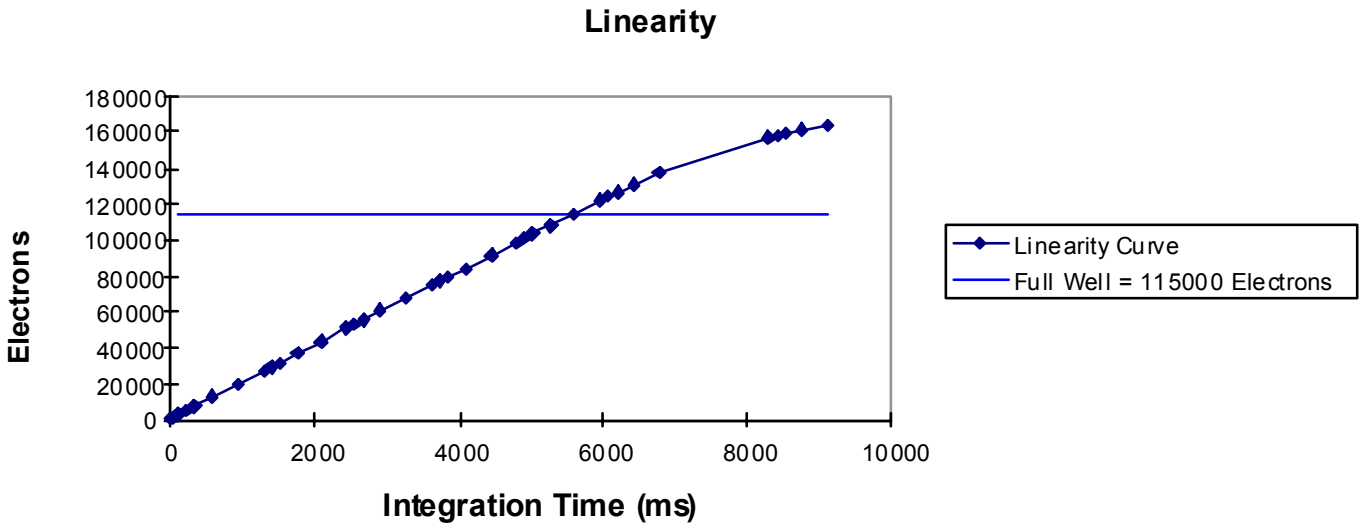


Figure 13: Measured Linearity
(Measurements taken using KAF-1600 sensor)

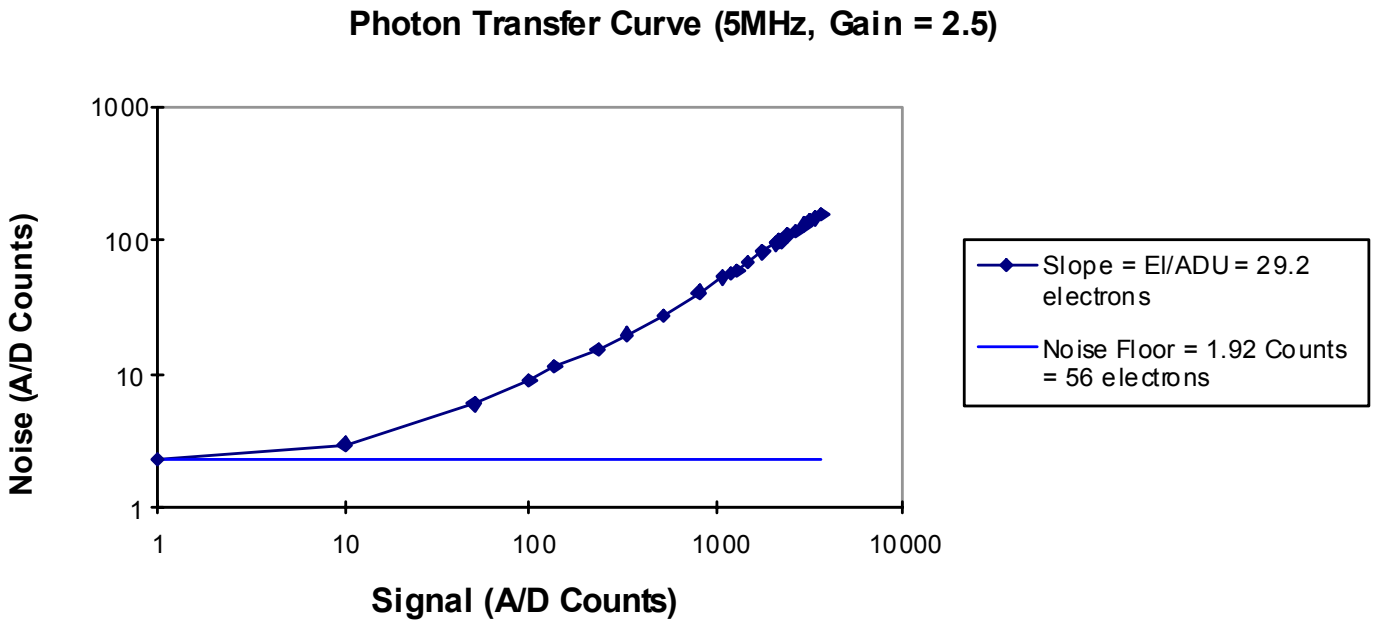


Figure 14: Measured Performance: Noise Floor
(Measurements taken using KAF-1600 sensor)

SYSTEM NOISE FLOOR VS. OPERATING FREQUENCY

Frequency (MHz)	Noise Floor (Electrons)	Dynamic Range* (Bits)	Dynamic Range* (dB)	EI/ADU	System Gain
1	40	11.49	69.17	29.2	2.5X
2	48	11.23	67.59	29.2	2.5X
3	50	11.17	67.23	29.2	2.5X
4	54	11.06	66.57	29.2	2.5X
5	56	11.00	66.25	29.2	2.5X
6	58	10.95	65.95	29.2	2.5X

Note: Dynamic Range Calculated using KAF1600 Sensor, Full Well = 115000 Electrons Measured

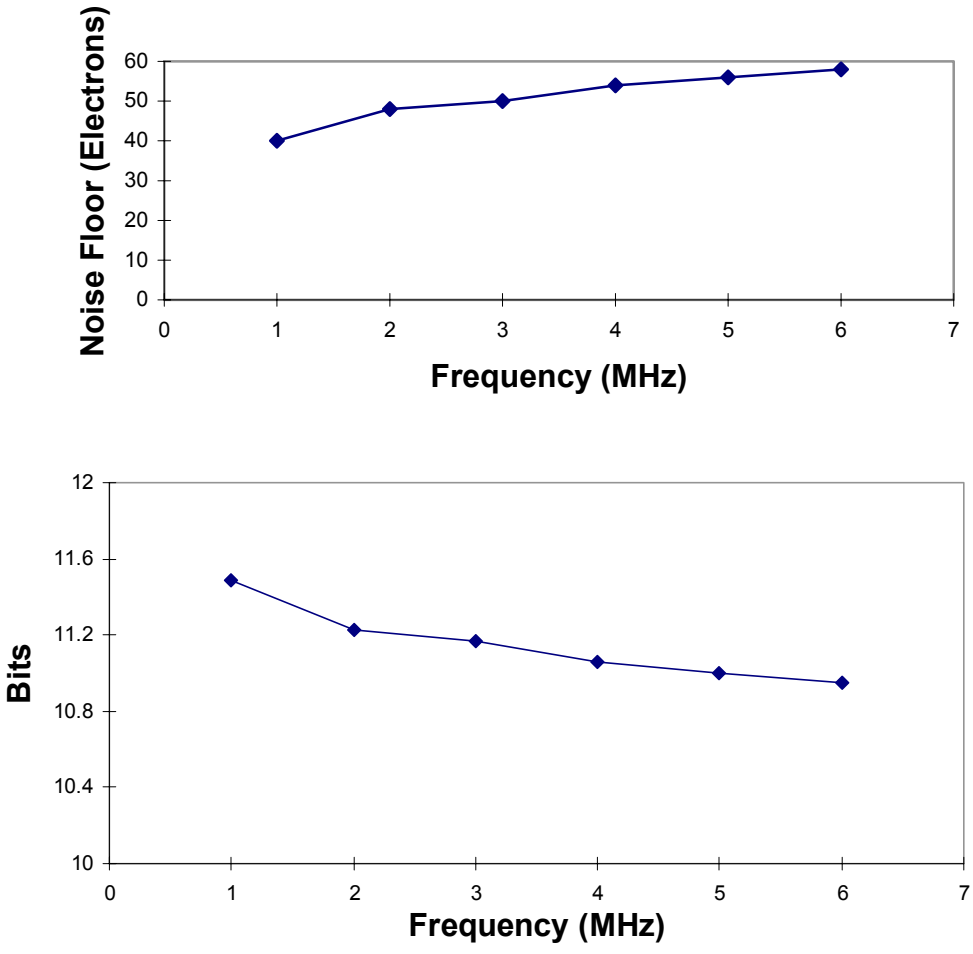


Figure 15: Measured Performance: Dynamic Range

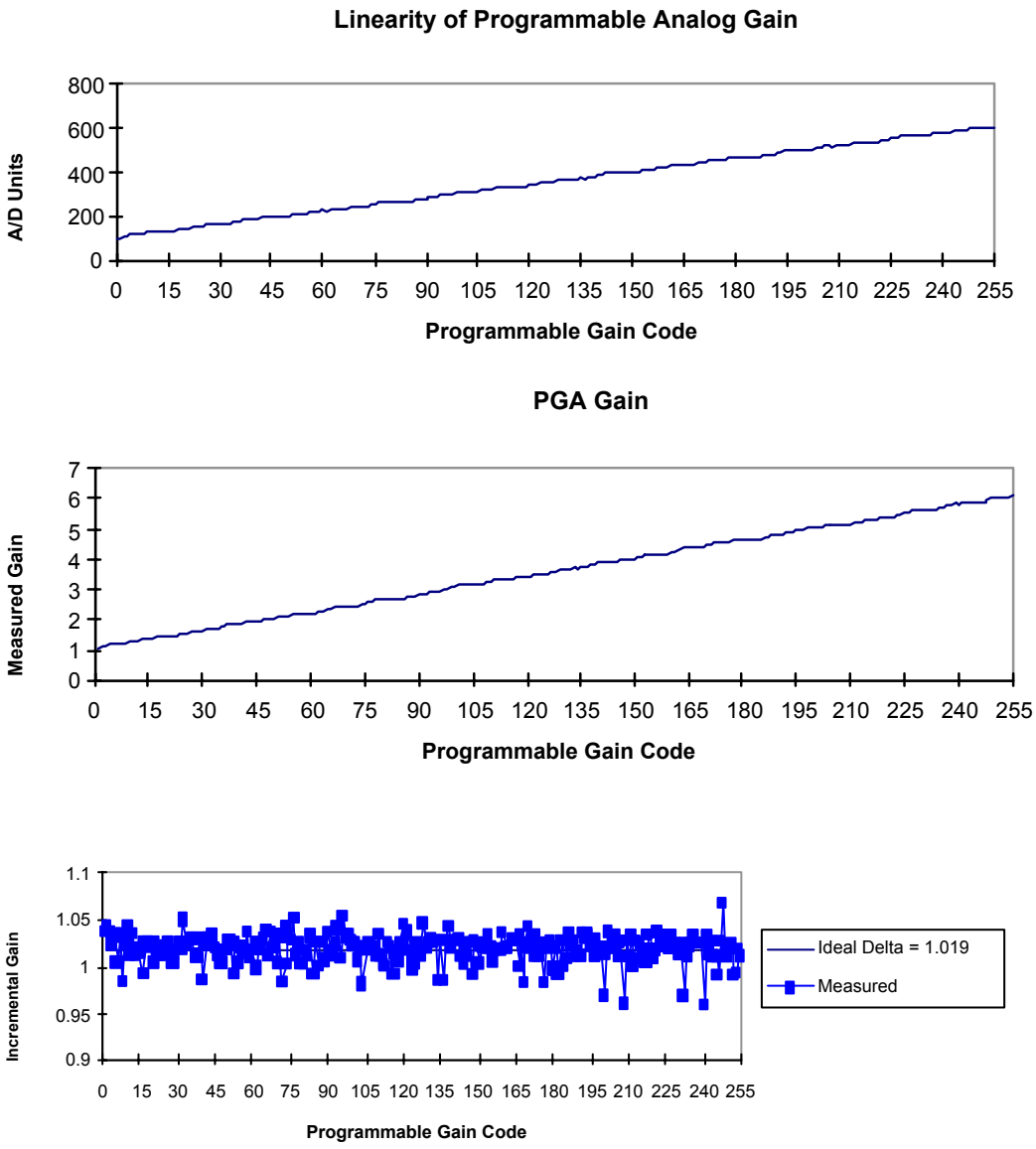


Figure 16: Measured Performance: A/D Programmable Gain

CONNECTOR PINOUTS

Imager Board Connectors J1, J2

Connector	Pin	Assignment
J1	1	N.C.
J1	2	VSUB
J1	3	N.C.
J1	4	VSUB
J1	5	N.C.
J1	6	VSUB
J1	7	VLG
J1	8	VSUB
J1	9	N.C.
J1	10	VSUB
J1	11	VDD
J1	12	VSUB
J1	13	VDD
J1	14	VSUB
J1	15	N.C.
J1	16	VSUB
J1	17	LOD/GAURD
J1	18	VSUB
J1	19	N.C.
J1	20	VSUB
J1	21	N.C.
J1	22	VSUB
J1	23	Neg 10V trace
J1	24	VSUB

Connector	Pin	Assignment
J2	1	VSUB
J2	2	RESET
J2	3	VSUB
J2	4	N.C.
J2	5	VSUB
J2	6	N.C.
J2	7	VSUB
J2	8	N.C.
J2	9	VSUB
J2	10	N.C.
J2	11	VSUB
J2	12	H2
J2	13	VSUB
J2	14	H1
J2	15	VSUB
J2	16	Video
J2	17	VSUB
J2	18	VOG
J2	19	VSUB
J2	20	VRD
J2	21	VSUB
J2	22	V2
J2	23	VSUB
J2	24	V1

Input Connector J6

Pin	Assignment	Pin	Assignment
1	INT0	2	GND
3	INT2	4	GND
5	INT3	6	GND
7	INT5	8	GND
9	IMAGE_ACQUIRE	10	GND
11	BIN0	12	GND
13	BIN1	14	GND
15	SCLOCK	16	GND
17	INT1	18	GND
19	SLOAD	20	GND
21	INT4	22	GND
23	BIN2	24	GND
25	SDATA	26	GND
27	STILL/FREE-RUN	28	GND
29	N.C.	30	GND
31	N.C.	32	GND
33	N.C.	34	GND

Output Connector J4

Connector	Pin	Assignment	Comment
J4	1	DIG0+	RS422
J4	2	DIG0-	RS422
J4	3	DIG1+	RS422
J4	4	DIG1-	RS422
J4	5	GND	
J4	6	DIG2+	RS422
J4	7	DIG2-	RS422
J4	8	DIG3+	RS422
J4	9	DIG3-	RS422
J4	10	GND	
J4	11	DIG4+	RS422
J4	12	DIG4-	RS422
J4	13	DIG5+	RS422
J4	14	DIG5-	RS422
J4	15	GND	
J4	16	DIG6+	RS422
J4	17	DIG6-	RS422
J4	18	DIG7+	RS422
J4	19	DIG7-	RS422
J4	20	GND	
J4	21	DIG8+	RS422
J4	22	DIG8-	RS422
J4	23	DIG9+	RS422
J4	24	DIG9-	RS422
J4	25	GND	
J4	26	DIG10+	RS422
J4	27	DIG10-	RS422
J4	28	DIG11+	RS422
J4	29	DIG11-	RS422
J4	30	GND	
J4	31	FRAME+	RS422
J4	32	FRAME-	RS422
J4	33	LINE+	RS422
J4	34	LINE-	RS422
J4	35	GND	
J4	36	PIX+	RS422
J4	37	PIX-	RS422
J4	38	N.C.	
J4	39	N.C.	
J4	40	N.C.	

Integrate Sync Connector J7

Connector	Pin	Assignment	Comment
J7	1	Integrate	TTL
J7	2	GND	

Power Connector J5

Connector	Pin	Assignment
J5	1	+18V
J5	2	SUPPLY GND
J5	3	-18V
J5	4	SUPPLY GND
J5	5	+5V

JTAG Connector J8

Connector	Pin	Assignment
J8	1	TCK
J8	2	GND
J8	3	TDO
J8	4	+5V
J8	5	TMS
J8	6	N.C.
J8	7	N.C.
J8	8	N.C.
J8	9	TDI
J8	10	GND

REFERENCES

Analog Devices AD9816 Specification Sheet

Linear Technology LT1372 Specification Sheet

KAF Series Device Performance Specifications

ISS Application Note on KAF Series Binning Mode Operation (DS 02-009)

ORDERING INFORMATION

The Kodak Digital Reference Evaluation Board may be ordered directly from:

Eastman Kodak Company,

Image Sensor Solutions

Rochester, NY 14650-2010

Tel. No. (585) 722-4385

Fax No. (585) 477-4947

Web: http://www.kodak.com/go/imagers

E-mail: imagers@kodak.com

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REVISION CHANGES

Revision No.	Description of Changes
6.0	Added Section 7.2.
7.0	Updated Table 2. Inserted new Table 3 and changed subsequent table numbers. Inserted new Figure 6 and changed subsequent figure numbers. Figure 8 (formerly Figure 7) caption changed - Frame Timing for KAF-3200ME. (KAF-16801E/LE removed because of new Figure 6.)

APPENDIX

APPENDIX1: PART NUMBER AVAILABILITY

Note:

This appendix may be updated independent of the performance specification.

Contact Eastman Kodak Company for the latest revision.

Evaluation Kit Number	Description	Supports
4H0081	KAF-0261 Reference Evaluation System	KAF-0261E
4H0077	KAF-0402 Reference Evaluation System	KAF-0402E, KAF-0402LE
4H0075	KAF-1301 Reference Evaluation System	KAF-1301E, KAF-1301LE
4H0074	KAF-1402 Reference Evaluation System	KAF-1402E
4H0078	KAF-1602 Reference Evaluation System	KAF-1602E, KAF-1602LE
4H0080	KAF-1001 Reference Evaluation System	KAF-1001E
4H0088	KAF-3200 Reference Evaluation System	KAF-3200E, KAF-3200ME
4H0076	KAF-4202 Reference Evaluation System	KAF-4202
4H0090	KAF-4301 Reference Evaluation System	KAF-4301E
4H0079	KAF-6303 Reference Evaluation System	KAF-6303E
4H0281	KAF-6302LE Reference Evaluation System	KAF-6303LE
4H0082	KAF-16801 Reference Evaluation System	KAF-16801E, KAF-16801LE

Digital Reference Evaluation Kit includes:

1. Timing Board (1)
2. Imager Board (1)
3. Power connector (1)
4. Connectors for digital input and frame grabber interface

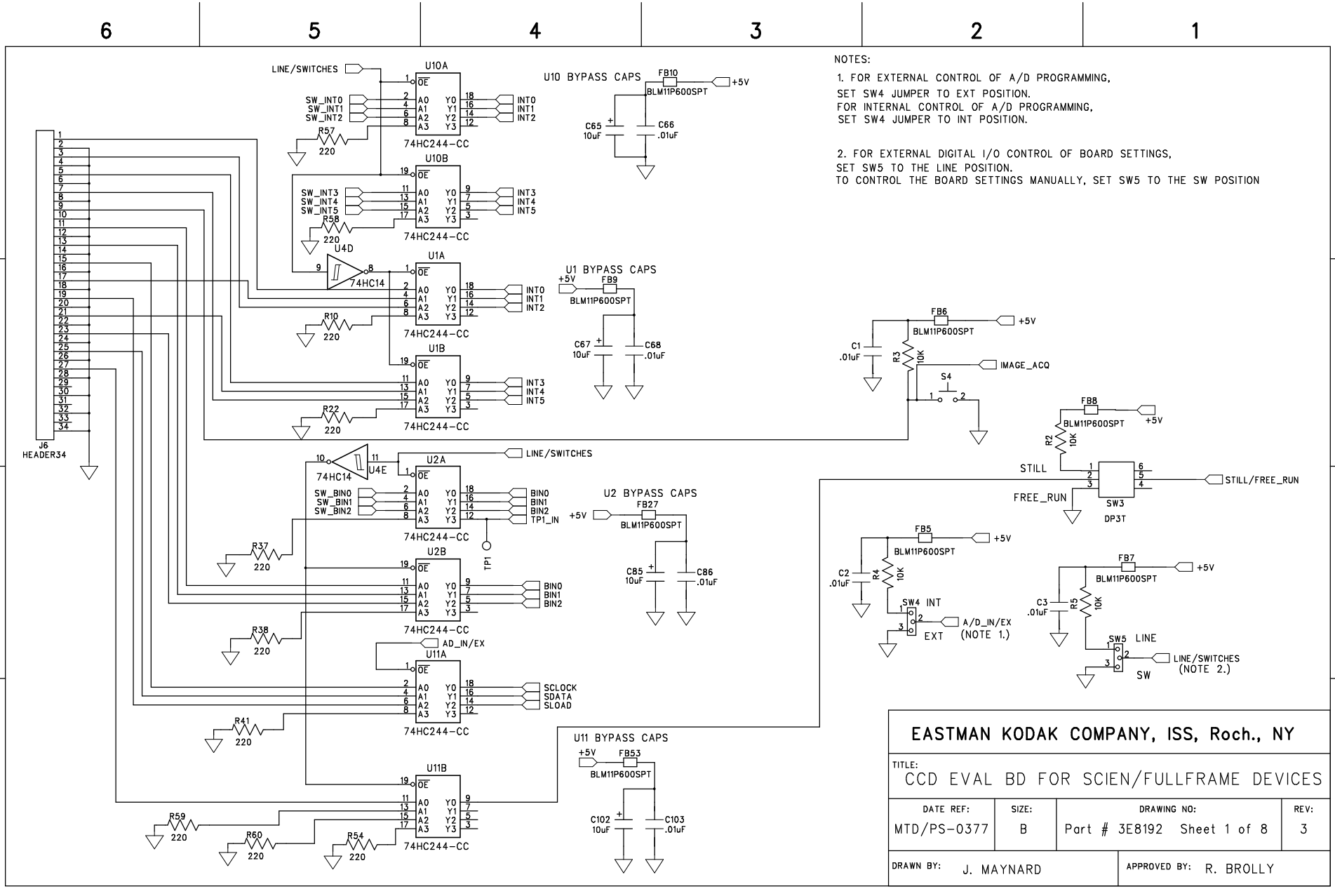
APPENDIX 2: PARTS LIST

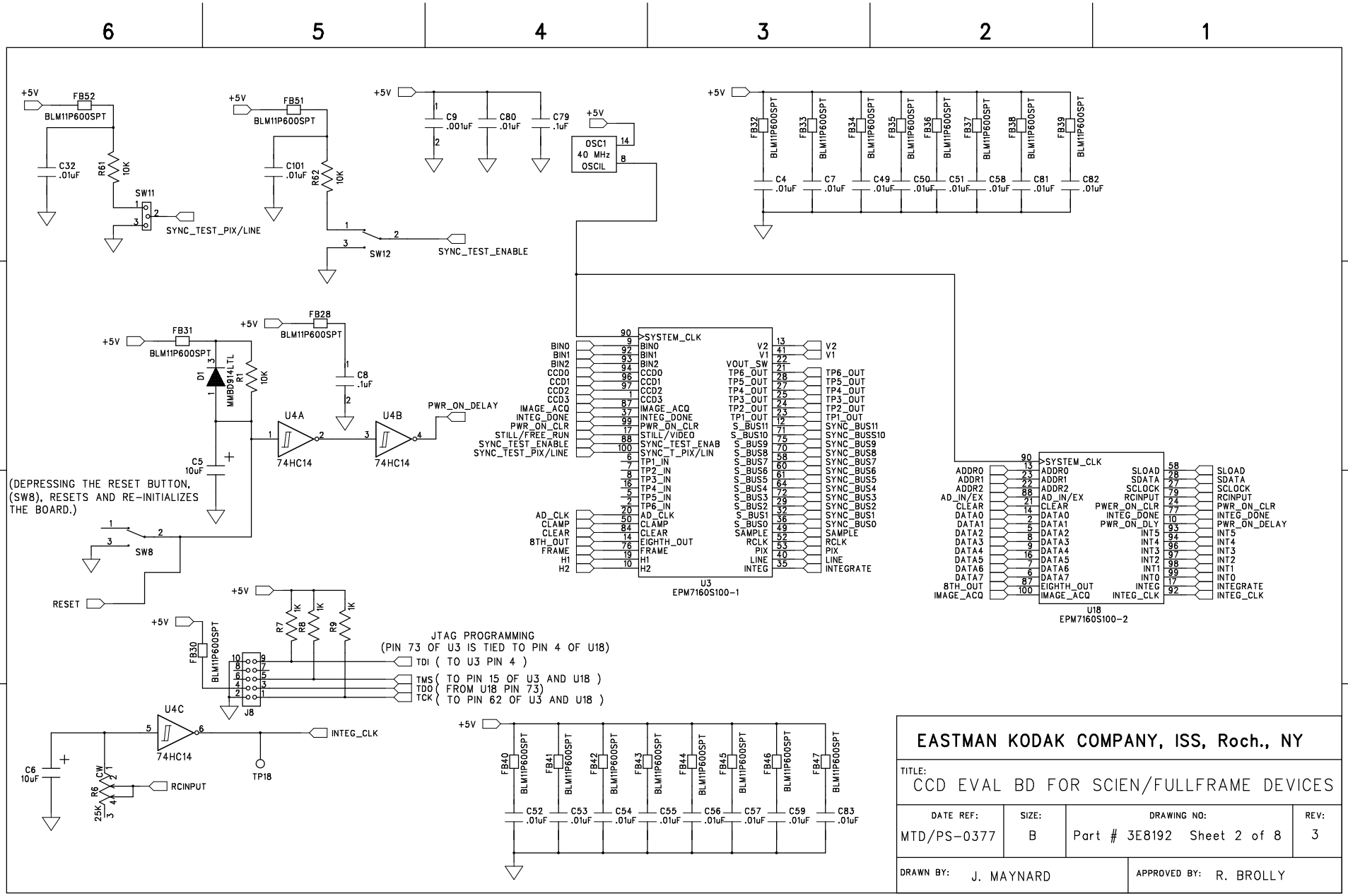
PART	DESCRIPTION	PACKAGE	QTY.	BOARD REFERENCE #	MANUFACTURER
BLM11P600SPT	FERRITE	FERRITE 0603	51	FB1-15, FB17-18, FB20-53	MURATA ERIE
06035A151JAT2A	150pF 50VDC	CAP 0603	1	C62	AVX
06035C102KAT4A	1000pF 50VDC	CAP 0603	3	C9, C43-44	AVX
08055A122KATMA	1200pF 50VDC	CAP 0805	3	C29, C91-92	AVX
06035C103KAT4A	.01uF 50VDC	CAP 0603	36	C1-4, C7, C31-32, C49-59, C66, C68, C70, C72, C74, C76-78, C80-83, C86, C94, C98, C100, C101, C103	AVX
0603YC104MAT4A	.1uF 16V	CAP 0603	13	C8, C10, C15, C30, C33, C35, C48, C79, C89, C93, C95, C97, C99	AVX
12063E334MATMA	0.33uF 25VDC	CAP 1206	2	C45-46	AVX
1206YC105MATRA	1uF 16VDC	CAP 1206	2	C90, C96	AVX
1206YG335ZATSA	3.3uF 16V	CAP 1206	6	C38-40, C42, C60, C64	AVX
TAJC475K035R	4.7uF 35VDC	CAP C CASE	3	C14, C106-107	AVX
TMC-MC1D106MTR	10 uF 20V	CAP C CASE	13	C5-6, C20, C34, C65, C67, C69, C71, C73, C75, C85, C88, C102	HITACHI
TPSE107M016S0125	100uF 16VDC	CAP E CASE	6	C28, C36, C37, C41, C61, C63	AVX
MMBD914LT1	DIODE	SOT-23	1	D1	MOTOROLA
MBRS130T3	DIODE	SMB	2	D9-10	MOTOROLA
HSMS-2805	DIODE	SOT-143	1	DP5	HEWLETT-PACKARD
MMBT100A	TRANSISTOR	SOT-23	1	Q1	FAIRCHILD
MMBT3640LT1	TRANSISTOR	SOT-23	1	Q2	MOTOROLA
	0 OHM	RES 0603	2	R14-15	
RK73H2AT1R0F	1 OHM 1%	RES 0805	1	R51	KOA SPEER
CRCW0805-5R1-JT	5.1 OHM 5%	RES 0805	2	R16, R18	DALE
CRCW0603-221-JT	220 OHM 5%	RES 0603	16	R10, R22, R36-38, R41, R43-47, R54,R57-60	DALE
CRCW0603-4750-FT	475 OHM 1%	RES 0603	1	R49	DALE
CRCW0603-102-JT	1K OHM 5%	RES 0603	5	R7-9, R19, R29	DALE
3266W-1-102	1K POT	THRU-HOLE	1	R17	BOURNS
CRCW0603-1501-FT	1.5K OHM 1%	RES 0603	1	R32	DALE
CRCW0603-222-JT	2.2K OHM 5%	RES 0603	1	R21	DALE
CRCW0603-332-JT	3.3K OHM 5%	RES 0603	1	R50	DALE
CRCW0603-6191-FT	6.19K OHM 1%	RES 0603	1	R34	DALE

CRCW0603-1002-FT	10K OHM 1%	RES 0603	25	R1-5, R20, R24-27, R30-31, R48, R52, R61-62, R64, R68, R70, R72-76, R78	DALE
4310R-101-103	10K SIP	10 POS THRU	1	R28	DALE
3266W-1-103	10K POT	THRU-HOLE	4	R11-13, R67	BOURNS
3296W-1-503	50K POT	THRU-HOLE	1	R6	BOURNS
CRCW0603-6982-FT	69.8K OHM 1%	RES 0603	1	R33	DALE
CRCW0603-8062-FT	80.6K OHM 1%	RES 0603	1	R35	DALE
CRCW0603-1003-FT	100K OHM 1%	RES 0603	2	R65-66	DALE
SN74HC244DW	OCTAL BUFF	SOL-20	4	U1-2, U10-11	TEXAS INSTRUMENTS
SN74HC14D	HEX INV	S0-14	1	U4	TEXAS INSTRUMENTS
SN74HC00D	NAND GATES	S0-14	1	U5	TEXAS INSTRUMENTS
SN74F574DW	DFF'S	SOL-20	2	U12-13	TEXAS INSTRUMENTS
AM26LS31CD	RS422 DRIVER	S0-16	4	U14-17	TEXAS INSTRUMENTS
LM7815CT	15V REG	TO-220	1	U19	NATIONAL
LM337T	NEG REG	TO-220	1	U22	NATIONAL
LT1372CS8		S0-8	1	U20	LINEAR TECHNOLOGY
EL7202CS	DRIVER	S0IC-8	2	U21, U24	ELANTEC
EPM7160STC100-10	EPLD	100 PIN TQFP	2	U3, U18	ALTERA
AD9816JS	A/D	QFP-44	1	U9	ANALOG DEVICES
C01100-40.000MHZ	CLOCK	14 PIN DIP	1	OSC1	Raltron
0555-015012027100	SINGLE PINS	THRU HOLE	4	OSC1 SOCKET PINS	MILL MAX
CTX33-3	INDUCTOR	SMT	1	L8	COILTRONICS
BNX002-01	PI FILTER	THRU-HOLE	3	L1-3	MURATA ERIE
BP08KT	8 POS DIP	THRU-HOLE	1	SW10	C&K
TPA11CGPC0	SWITCH	SPST	2	S4, SW8	AUGAT
94HCB16	HEX SWITCH	HEX SW	1	SW1	GRAYHILL
94HCB08	OCTAL SWITCH	OCTAL SW	4	SW2, SW6-7, SW9	GRAYHILL
1101M2S3CBE2	SWITCH	on-none-on	1	SW12	C&K
1103M2S3CBE2	SWITCH	on-off-on	1	SW3	C&K
947701-01	SWITCH KNOB	KNOB	5		GRAYHILL
SL90-5 (123506)	BOARD MOUNT	5 PIN PWR	1	J5	WEIDMULLER
BL5 (125946)	PLUG CONNECTOR	5 PIN PWR	1		WEIDMULLER
5-826632-0	BREAKAWAY STRIP	HEADER 40	1	J4	AMP
636-4041	40 PIN CONNECTOR	FEMALE	1		T&B
5-826632-0	BREAKAWAY STRIP	HEADER 34	1	J6	AMP
636-3441	34 PIN CONNECTOR	FEMALE	1		T&B

5-826632-0	BREAKAWAY STRIP	HEADER 24	2	J1,J2	AMP
5-826632-0	BREAKAWAY STRIP	HEADER 10	1	J8	AMP
5-826632-0	BREAKAWAY STRIP	HEADER 2	1	J7	AMP
5-826632-0	BREAKAWAY STRIP	JUMPER	9	JMP1, JMP3-7, SW4-5, SW11	AMP
5-826926-0	BREAKAWAY STRIP	TEST POINT	27	TP1, TP4-5, TP10, TP12, TP14-17, TP22, TP24-28, TP31-39, TP44-46	AMP

APPENDIX 3: IMAGER BOARD SCHEMATICS


6
5
4
3
2
1
D
C
B
A
NOTES:
1. FOR EXTERNAL CONTROL OF A/D PROGRAMMING,
SET SW4 JUMPER TO EXT POSITION.
FOR INTERNAL CONTROL OF A/D PROGRAMMING,
SET SW4 JUMPER TO INT POSITION.
2. FOR EXTERNAL DIGITAL I/O CONTROL OF BOARD SETTINGS,
SET SW5 TO THE LINE POSITION.
TO CONTROL THE BOARD SETTINGS MANUALLY, SET SW5 TO THE SW POSITION
J6
HEADER34
U10A
U10B
U4D
74HC14
U1A
U1B
74HC244-CC
LINE/SWITCHES
SW_INT0
SW_INT1
SW_INT2
SW_INT3
SW_INT4
SW_INT5
INT0
INT1
INT2
INT3
INT4
INT5
R57
R58
R10
R22
220
U10 BYPASS CAPS
U1 BYPASS CAPS
FB10
FB9
BLM11P600SPT
+5V
C65
10uF
C66
.01uF
C67
C68
U4E
U2A
U2B
U11A
U11B
SW_BIN0
SW_BIN1
SW_BIN2
BIN0
BIN1
BIN2
TP1_IN
TP1
AD_IN/EX
SCLOCK
SDATA
SLOAD
R37
R38
R41
R59
R60
R54
U2 BYPASS CAPS
FB27
C85
C86
U11 BYPASS CAPS
FB53
C102
C103
FB6
C1
.01uF
R3
10K
IMAGE_ACQ
S4
FB8
R2
STILL
FREE_RUN
STILL/FREE_RUN
SW3
DP3T
FB5
C2
R4
SW4 INT
EXT
A/D_IN/EX
(NOTE 1.)
FB7
C3
R5
SW5 LINE
SW
LINE/SWITCHES
(NOTE 2.)
EASTMAN KODAK COMPANY, ISS, Roch., NY
TITLE:
CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES
DATE REF:
MTD/PS-0377
SIZE:
B
DRAWING NO:
Part # 3E8192 Sheet 1 of 8
REV:
3
DRAWN BY:
J. MAYNARD
APPROVED BY:
R. BROLLY



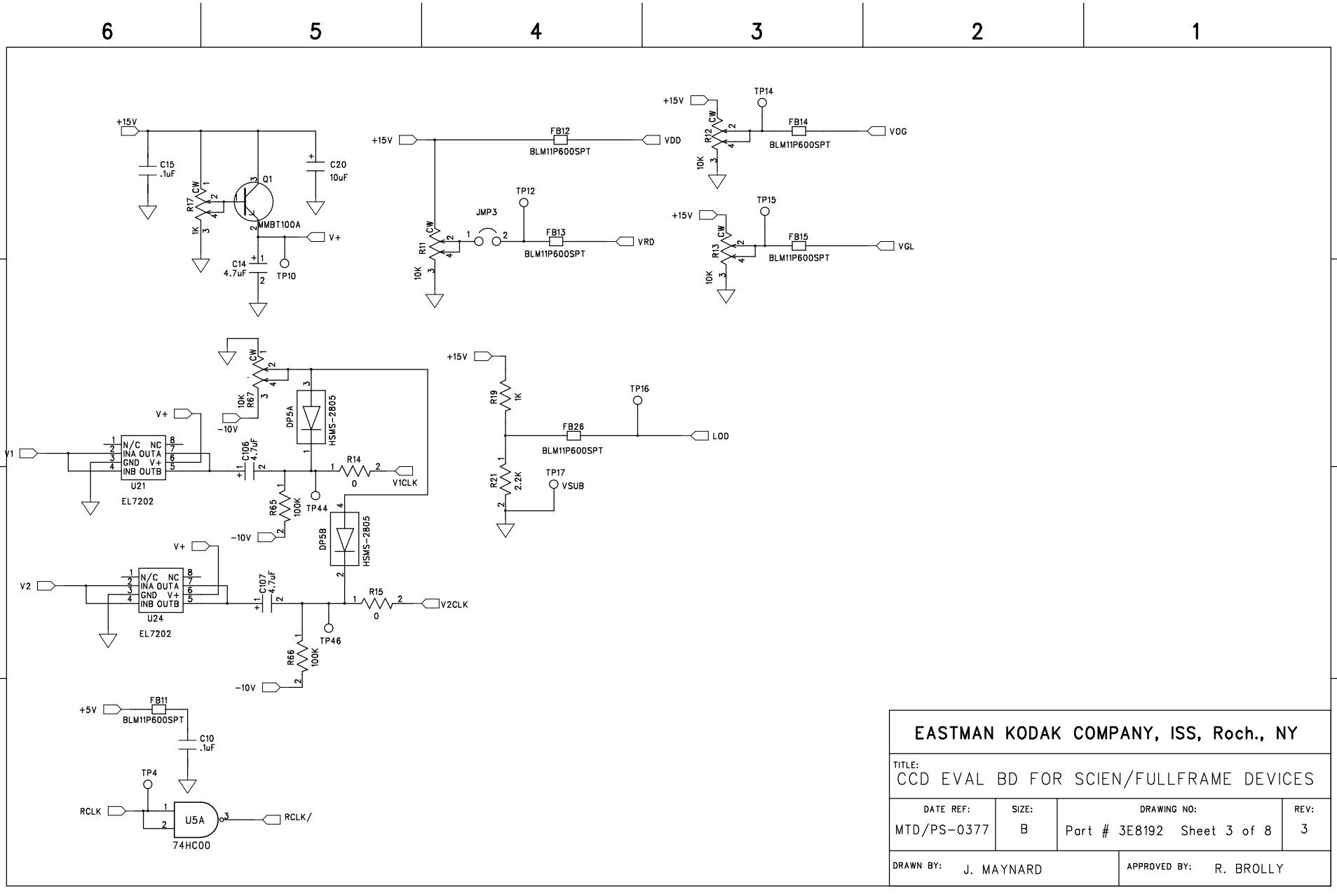
EASTMAN KODAK COMPANY, ISS, Roch., NY

TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES

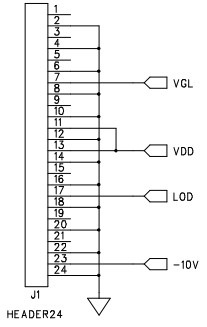
DATE REF:	SIZE:	DRAWING NO:	REV:
MTD/PS-0377	B	Part # 3E8192 Sheet 2 of 8	3

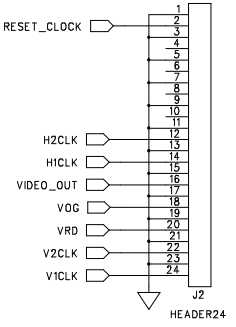
DRAWN BY: J. MAYNARD

APPROVED BY: R. BROLLY

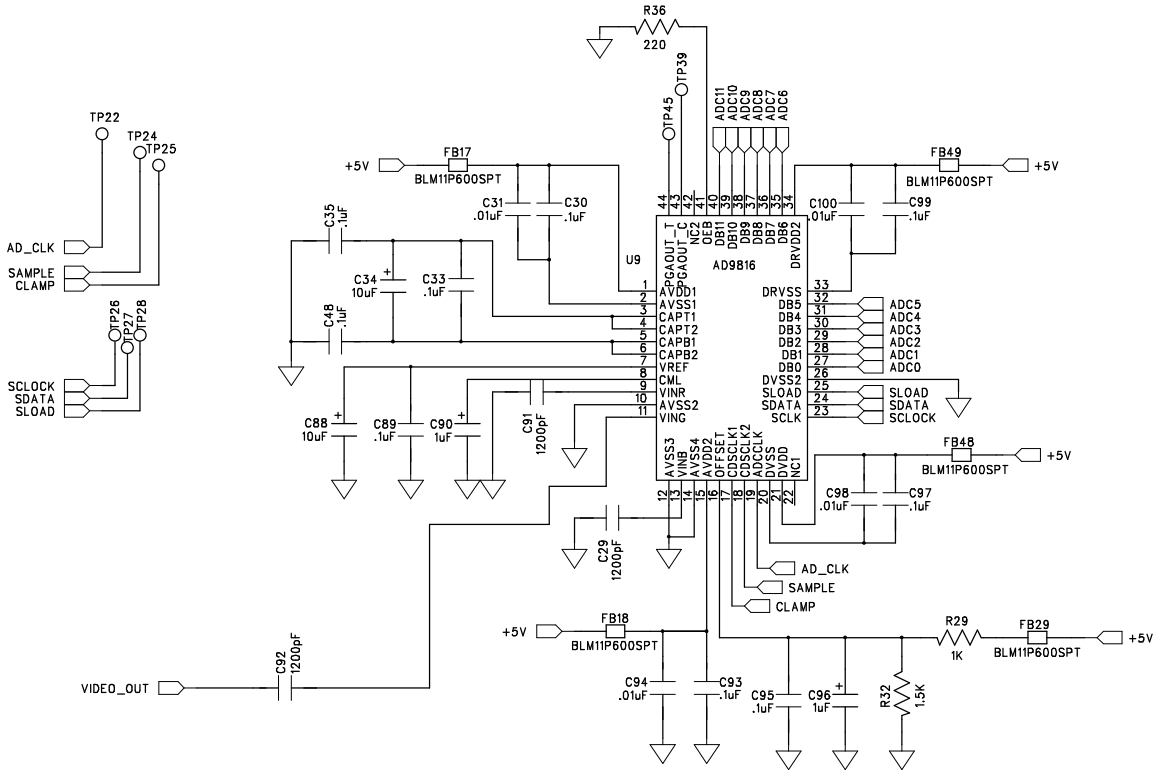


EASTMAN KODAK COMPANY, ISS, Roch., NY			
TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES			
DATE REF: MTD/PS-0377	SIZE: B	DRAWING NO: Part # 3E8192 Sheet 3 of 8	REV: 3
DRAWN BY: J. MAYNARD		APPROVED BY: R. BROLLY	

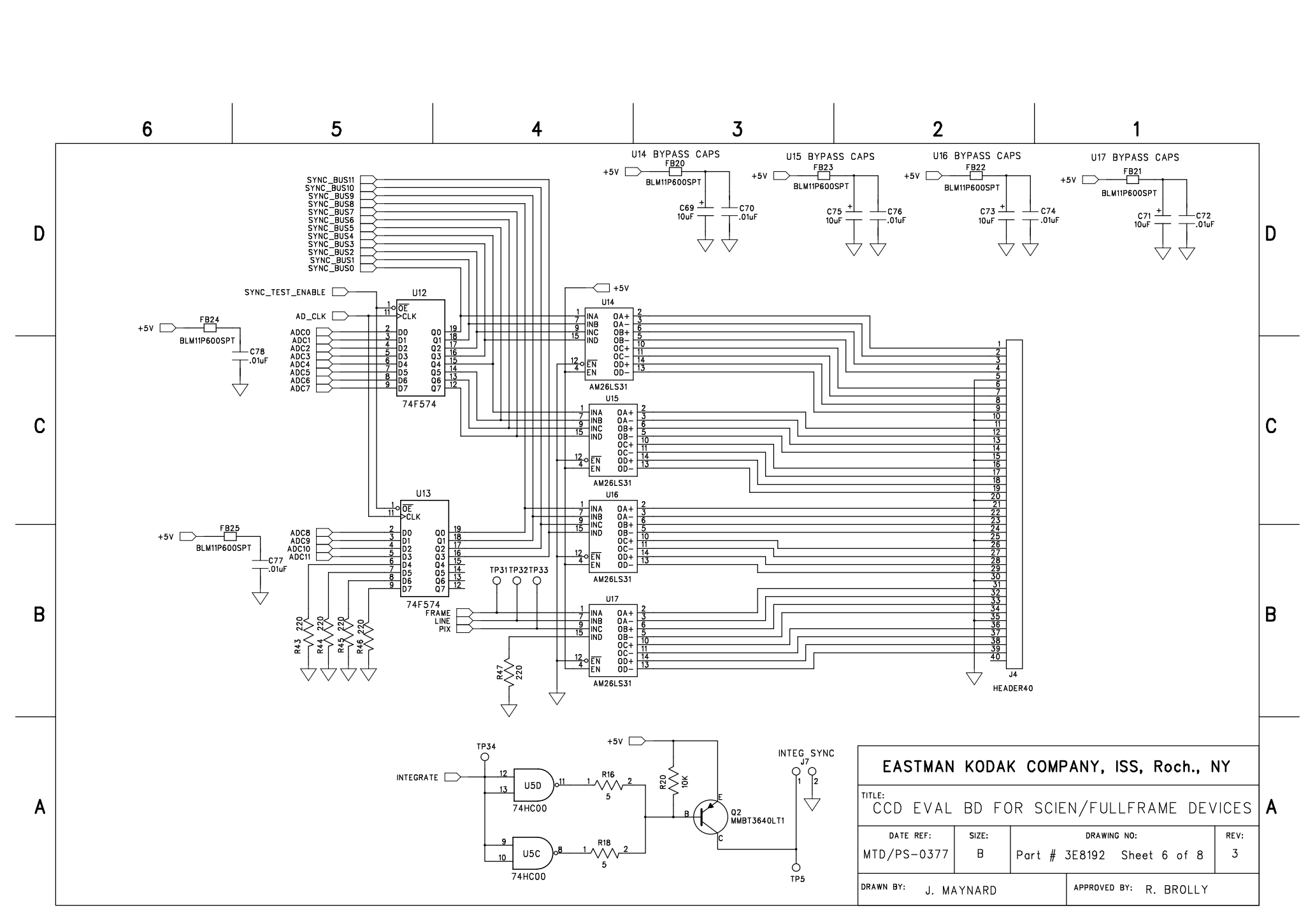




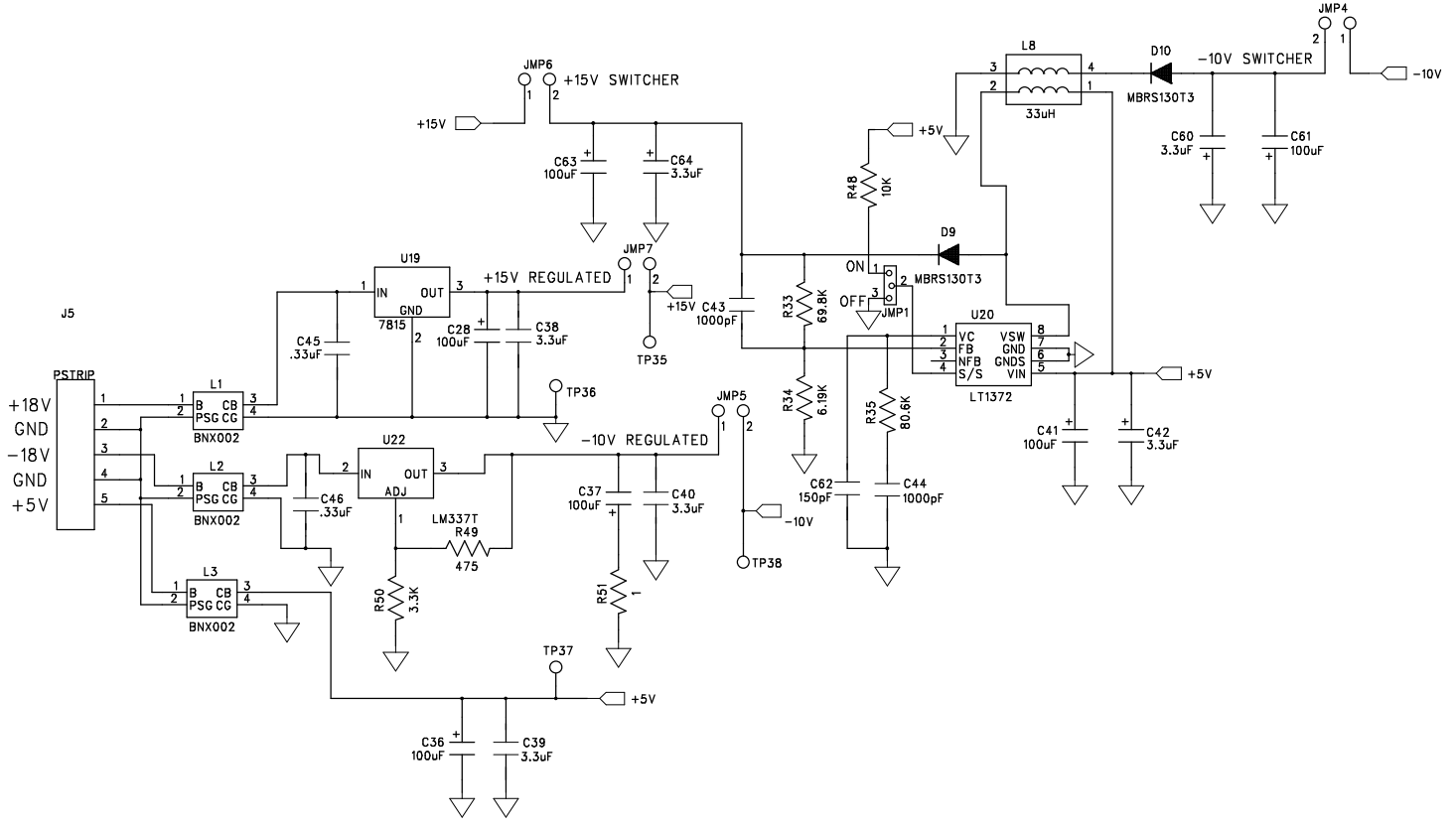
EASTMAN KODAK COMPANY, ISS, Roch., NY			
TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES			
DATE REF: MTD/PS-0377	SIZE: B	DRAWING NO: Part # 3E8192 Sheet 4 of 8	REV: 3
DRAWN BY: J. MAYNARD		APPROVED BY: R. BROLLY	



EASTMAN KODAK COMPANY, ISS, Roch., NY			
TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES			
DATE REF: MTD/PS-0377	SIZE: B	DRAWING NO: Part # 3E8192 Sheet 5 of 8	REV: 3
DRAWN BY: J. MAYNARD		APPROVED BY: R BROLLY	



EASTMAN KODAK COMPANY, ISS, Roch., NY			
TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES			
DATE REF: MTD/PS-0377	SIZE: B	DRAWING NO: Part # 3E8192 Sheet 6 of 8	REV: 3
DRAWN BY: J. MAYNARD		APPROVED BY: R. BROLLY	

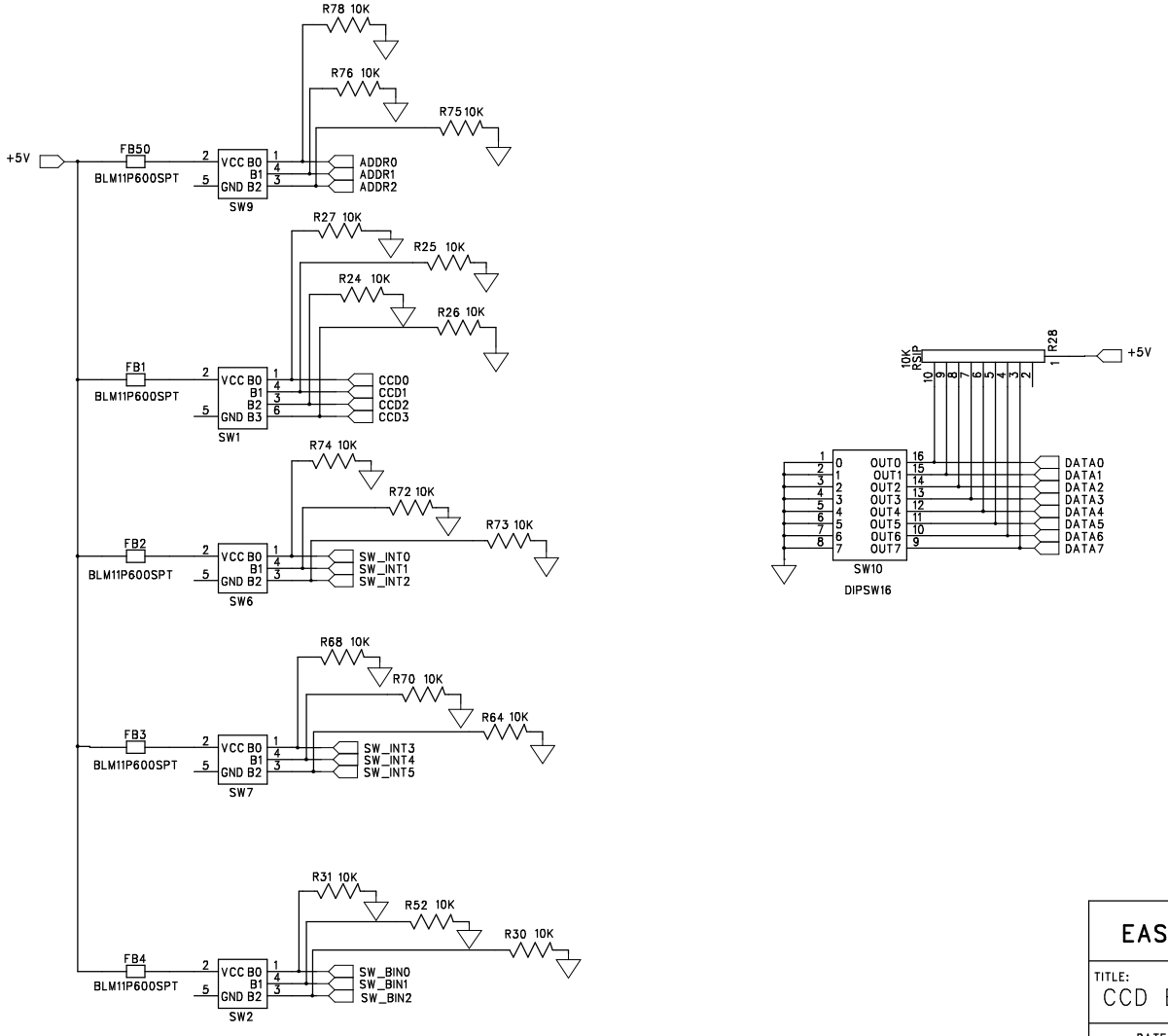


NOTES:

1. TO UTILIZE SWITCHING POWER SUPPLY, U20, SET JMP1 TO ON POSITION. INSTALL JMP 4 AND JMP 6 . REMOVE JMP 5 AND JMP 7.

2. WHEN UTILIZING 3 EXTERNAL SUPPLIES, SET JMP 1 TO OFF POSITION, REMOVE JMP 4 AND JMP 6. INSTALL JMP 5 AND JMP 7.

EASTMAN KODAK COMPANY, ISS, Roch., NY			
TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES			
DATE REF: MTD/PS-0377	SIZE: B	DRAWING NO: Part # 3E8192 Sheet 7 of 8	REV: 3
DRAWN BY: J. MAYNARD		APPROVED BY: R. BROLLY	



EASTMAN KODAK COMPANY, ISS, Roch., NY

TITLE: CCD EVAL BD FOR SCIEN/FULLFRAME DEVICES

DATE REF:	SIZE:	DRAWING NO:	REV:
MTD/PS-0377	B	Part # 3E8192 Sheet 8 of 8	3

DRAWN BY: J. MAYNARD

APPROVED BY: R. BROLLY

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